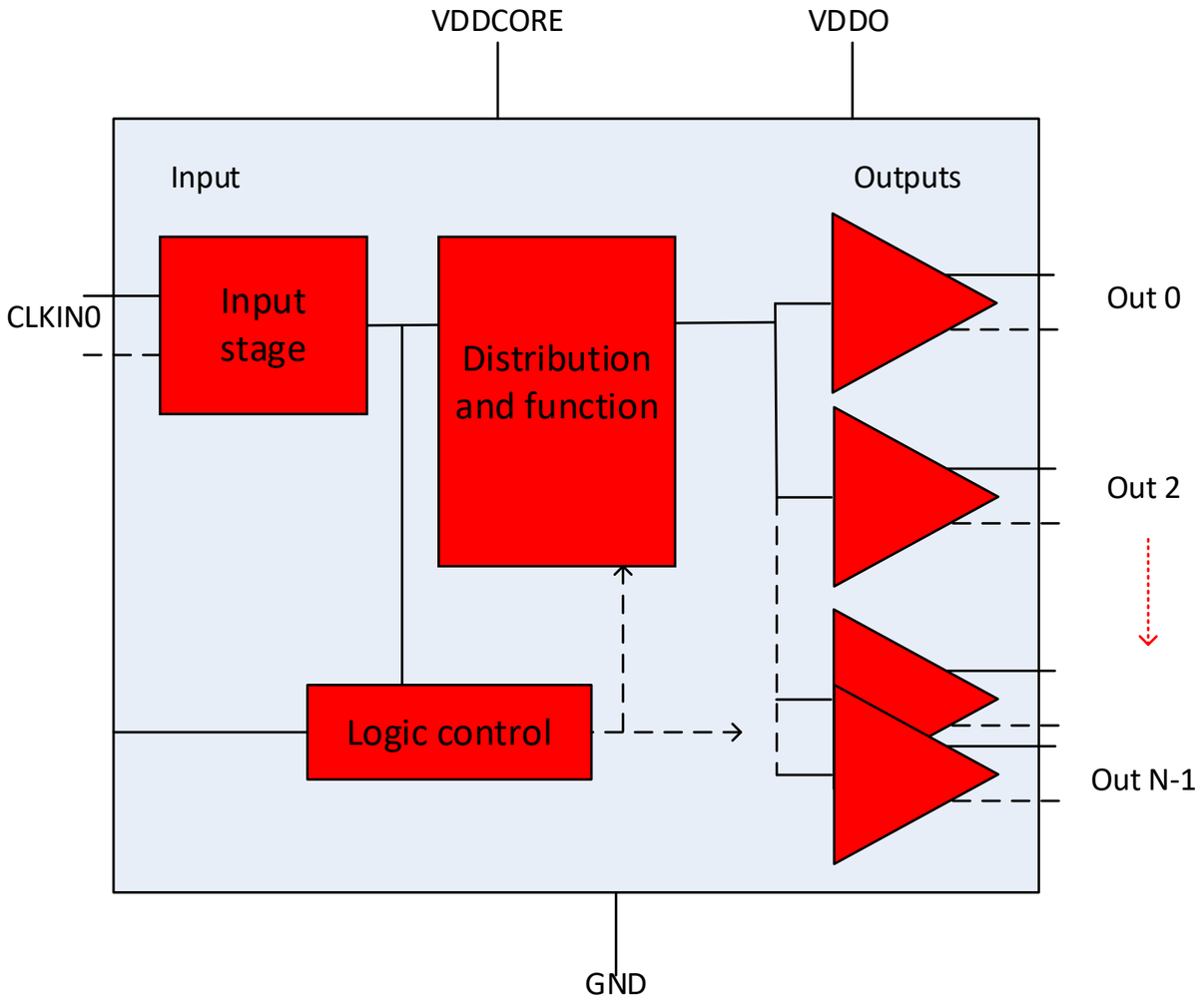
Clock Buffers: Key parameters and Specifications

TI Precision Labs – Clocks and Timing

Prepared by Badarish Colathur Arvind

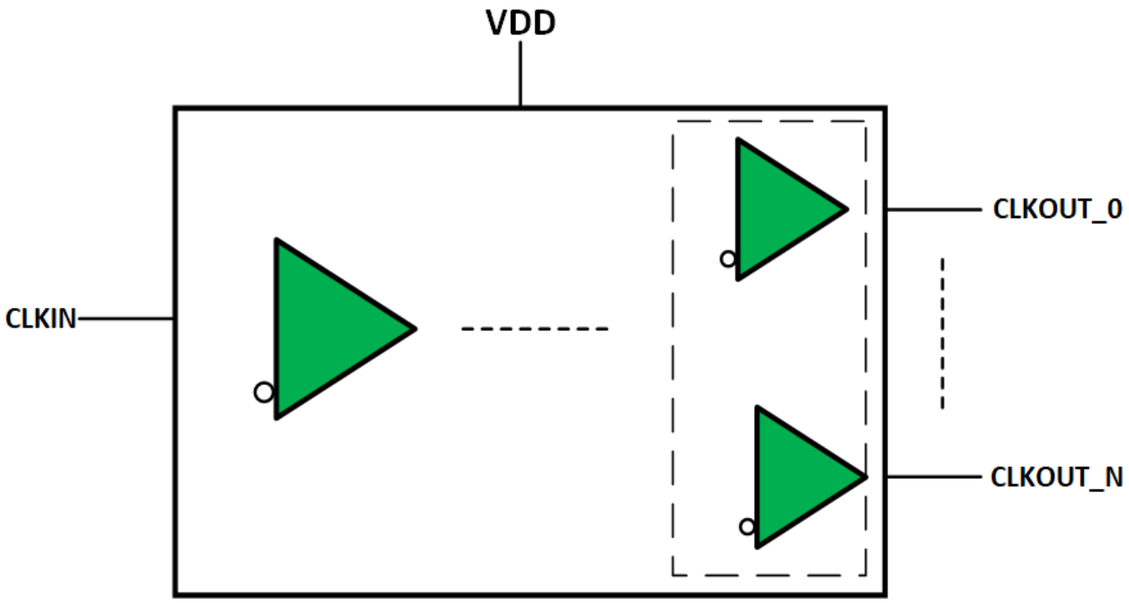
Presented by Liam Keese

Clock buffer overview

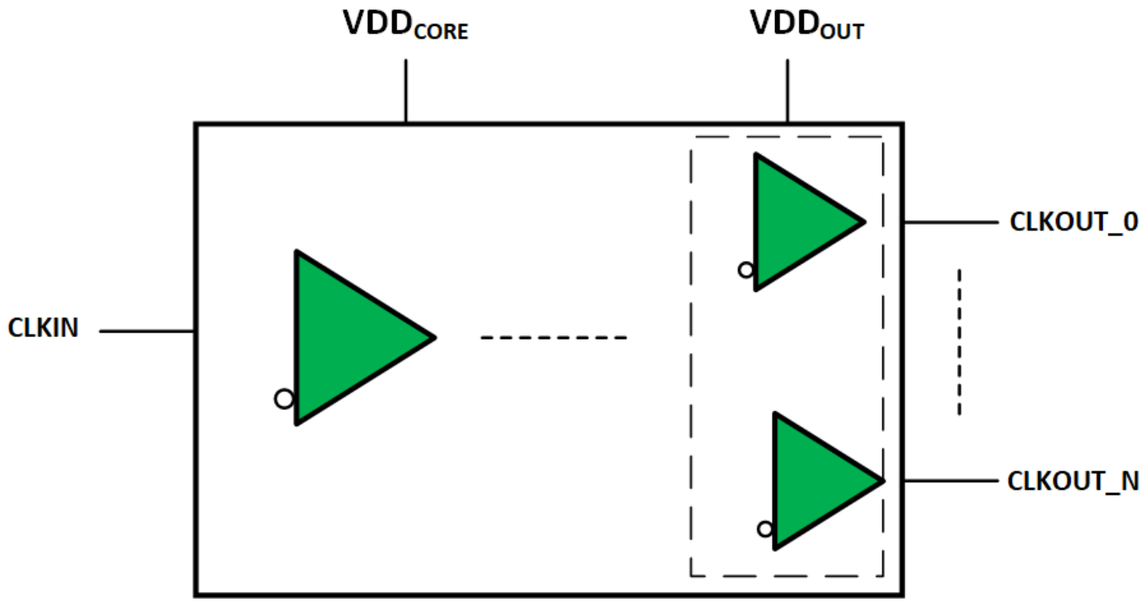


Clock buffer voltage supply

Single Supply



Dual Supply



Clock buffer input/output format

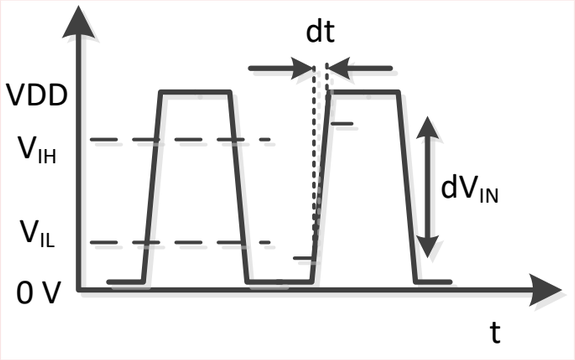
	Single-ended	Differential
Signal format	CMOS, LVTTL, Sine	LVDS, LVPECL, HCSL, CML
Routing	Simple	differential traces need to be matched
Components	Fewer	~2x single-ended
Noise coupling	Prone to noise-coupling	Provides common mode noise rejection/coupling

Clock buffer input configuration

Single-ended

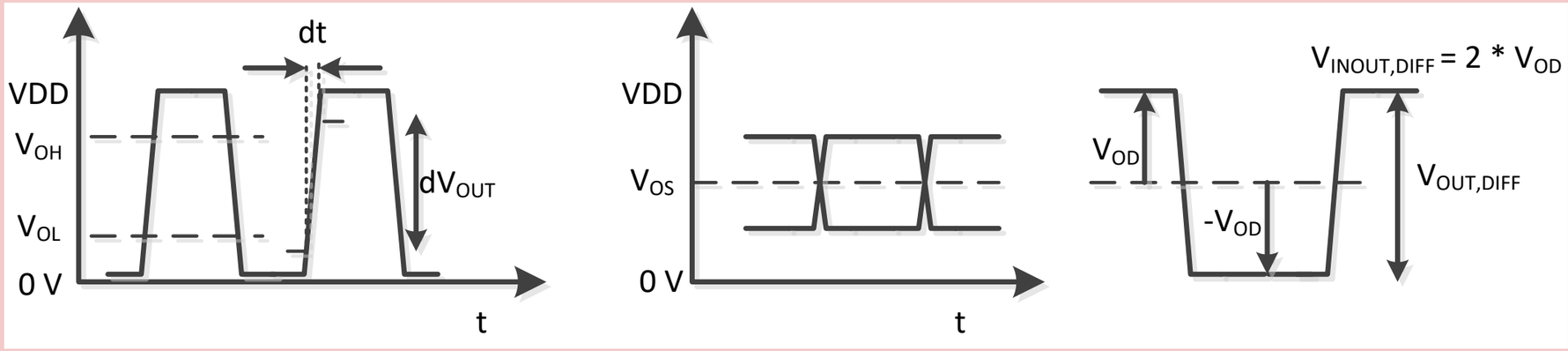
A typical single ended specification looks like the one shown below from LMK1C1104:

CLOCK INPUT					
f_{IN_SE}	Input frequency	V_{DD} = 3.3 V	DC	250	MHz
		V_{DD} = 2.5 V and 1.8 V	DC	200	
V_{IH}	Input high voltage		0.7 x V_{DD}		V
V_{IL}	Input low voltage			0.3 x V_{DD}	
dV_{IN}/dt	Input slew rate	20% - 80% of input swing	0.1		V/ns
I_{IN_LEAK}	Input leakage current		–50	50	uA
C_{IN_SE}	Input capacitance	at 25°C		7	pF



Clock buffer output level specifications

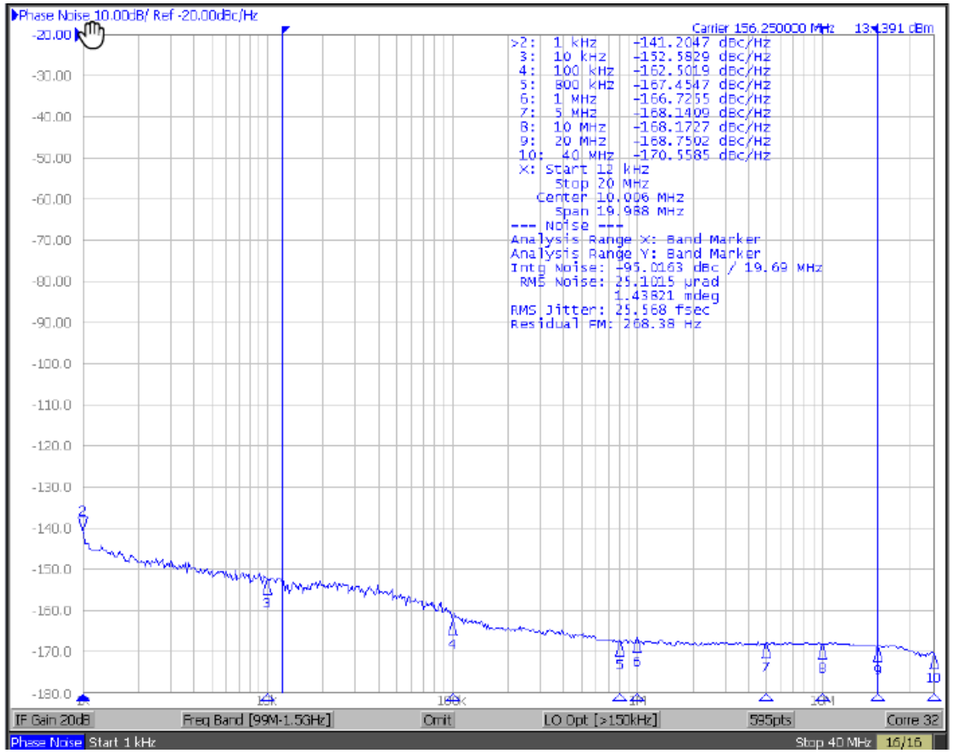
Signal type	VOH	VOL	$V_{OUT, DIFF}$ (2*VOD)	VOS (Output Common-mode)	R_{OUT}



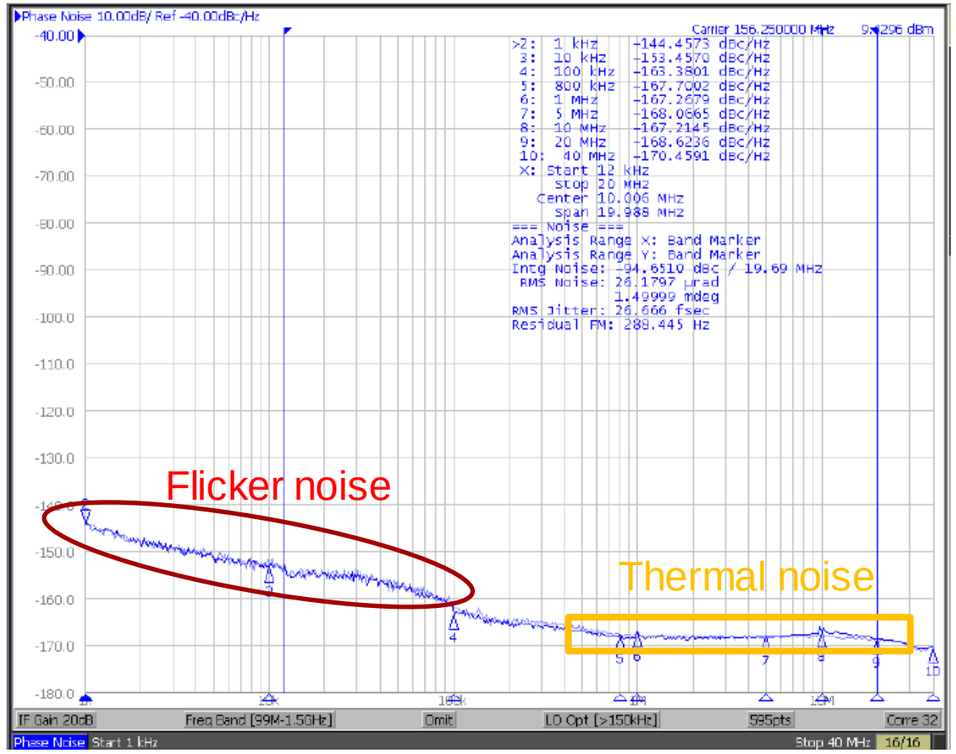
Clock buffer output level specifications

Signal type	VOH	VOL	$V_{OUTDIFFP-P}$ (2*VOD)	VOS (Output Common-mode)	R_{OUT}
Single-ended: CMOS	0.7*VDD	0.3*VDD	VDD	0.5*VDD	50 Ω (But not all devices have it)
Differential: LVDS	1.365 V	1.015 V	700 mV	1.2 V	High impedance
Differential: LVPECL	VDD – 1 V	VDD – 1.8 V	1.6 V	VDD – 1.4 V	Low impedance
Differential: HCSL	700 mV	0 V	1.4 V	350 mV	High impedance
Differential: CML	VDD	VDD – 0.4 V	800 mV	VDD – 0.2 V	50 Ω

Clock buffer jitter and phase noise



Input clock phase noise @156.25 MHz

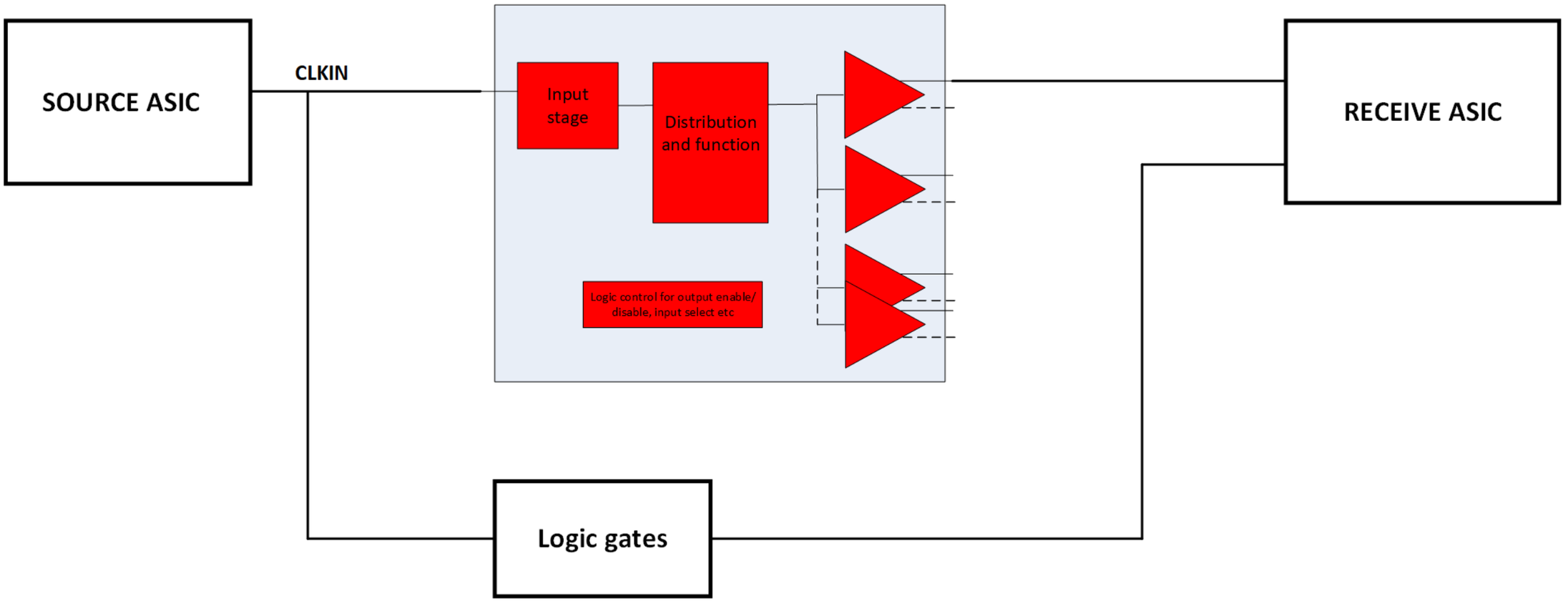


Output clock phase noise. The jitter added by the buffer is due to its flicker noise and thermal noise components.

Clock buffer jitter and phase noise

	Output Peak to Peak Swing	Input Slew rate	Additive jitter/Phase noise	Summary
CMOS	VDD	High	1st (Best)	Best noise performance due to high peak to peak swing.
LVPECL	1.6 V	High	2nd	Noise performance is very good due to high swing.
HCSL	1.4 V	High	3rd	Noise performance not as good as LVPECL due to slightly lower swing.
LVDS	700 mV	Low	4th	Noise performance limited due to low swing and slew rate.

Clock buffer propagation delay



- The various stages of a buffer contribute to propagation delay (t_{PD})
- The input stage and output stage contribute less than the middle stage.

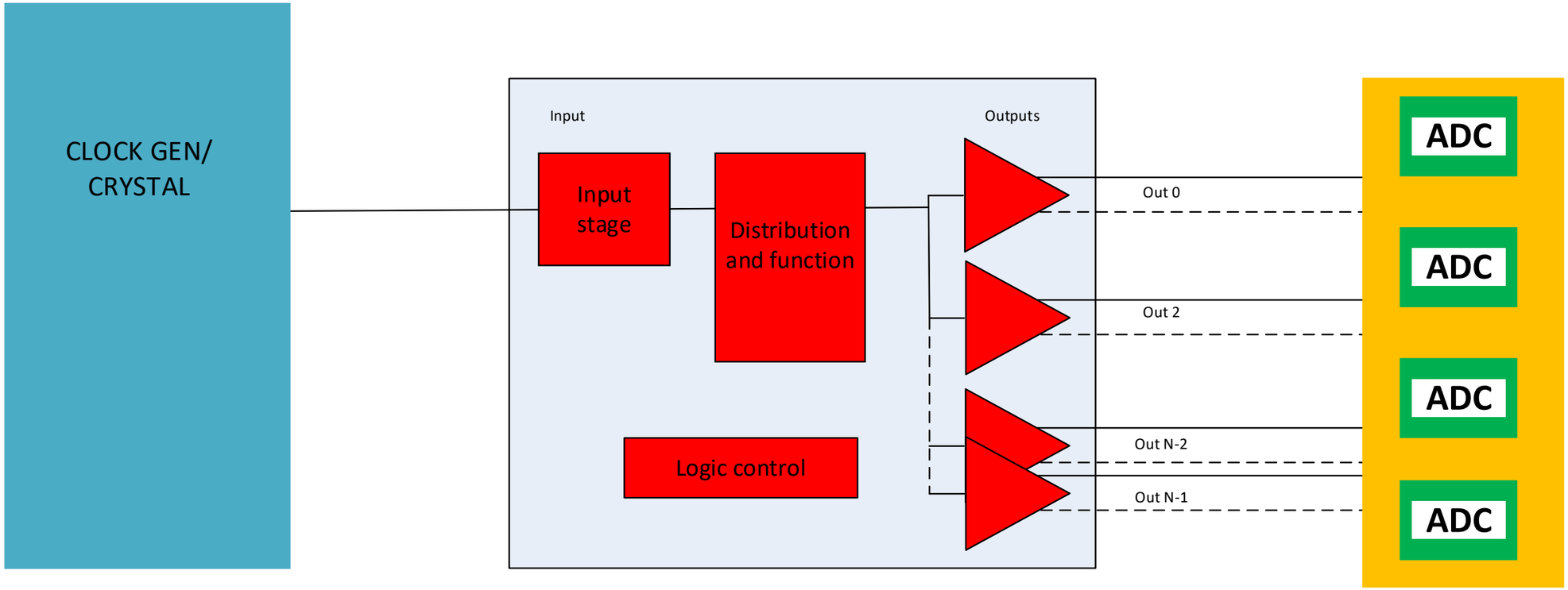
Clock buffer propagation delay

	Value	Mean	Min	Max	St Dev	Count	Info
C4C1 Dely	10.77ns	10.764203n	10.74n	10.78n	8.068p	180.0	
C4C2 Dely	10.81ns	10.804691n	10.78n	10.83n	7.115p	180.0	
C4C3 Dely	10.79ns	10.800242n	10.78n	10.83n	10.41p	180.0	
C1 Rise	258.8ps	275.86701p	220.7p	355.2p	22.32p	180.0	
C4 Freq	50.17MHz	50.158705M	50.08M	50.22M	24.5k	180.0	
C4 Ampl*	3.3V	3.3092805	3.26	3.36	18.05m	180.0	
C1 Ampl	1.5V	1.4931166	1.458	1.56	22.55m	180.0	
C2C1 Dely	-33.09ps	-40.488365p	-68.35p	-14.17p	8.609p	180.0	

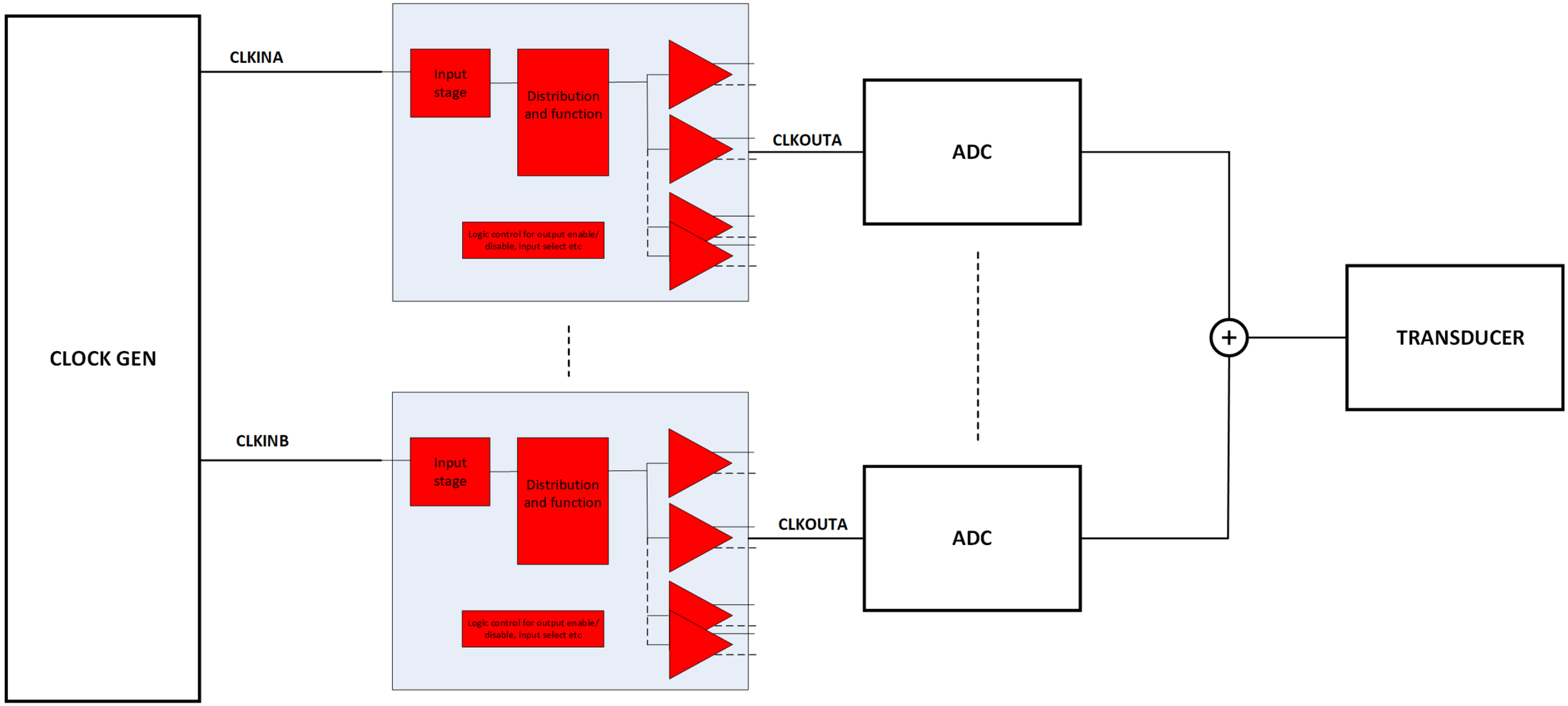
Input

Outputs

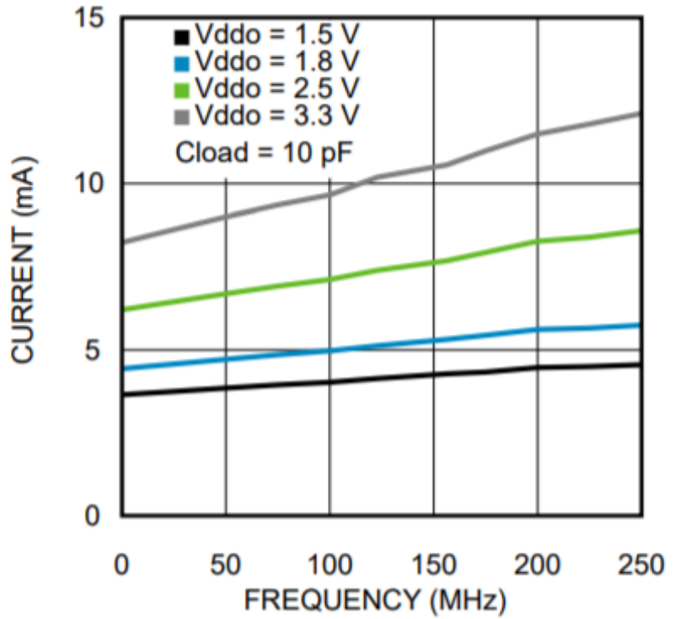
Clock buffer channel-channel skew



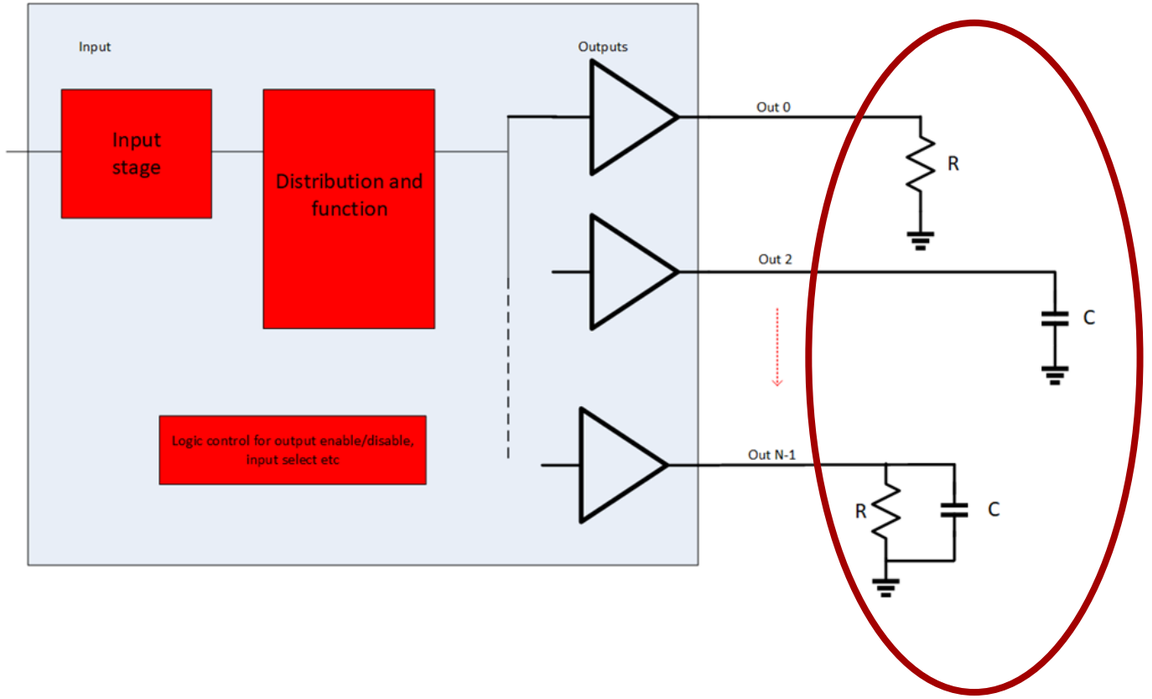
Clock buffer part to part skew



Clock buffer power consumption and loading



Current consumption vs. frequency, Cload = 10pF



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Clock Buffers: Key Parameters and Specifications - Quiz

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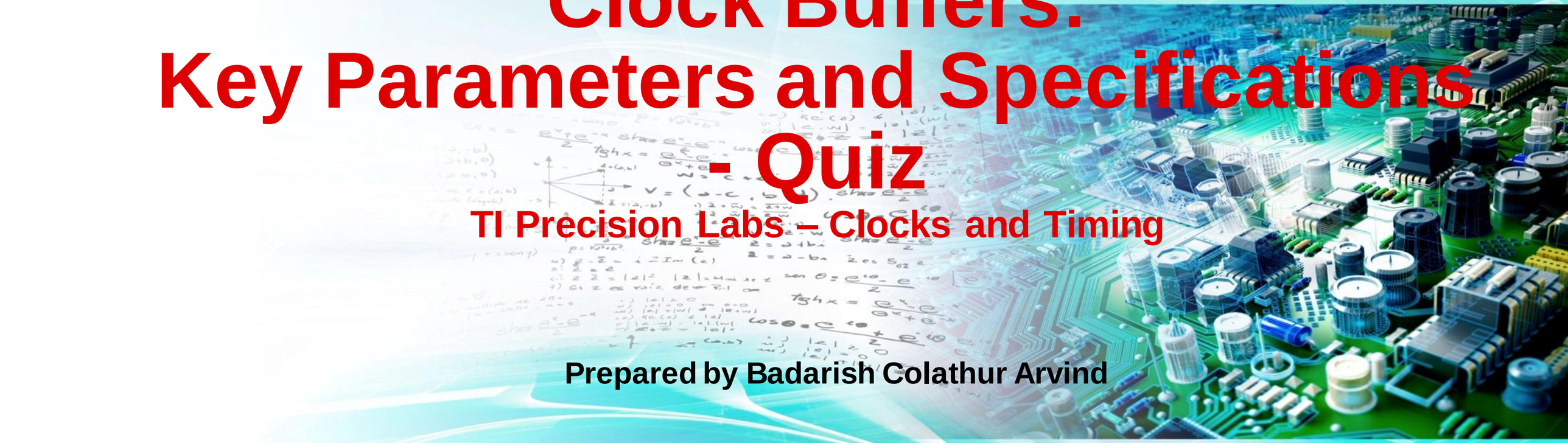

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Quiz

- True or false: Single ended buffers are immune to external noise coupling
- True or false: For a given VDD, CMOS buffers provide the highest output amplitude
- True or false: Increasing the input slew rate and input amplitude reduces the output additive jitter of the buffer
- True or false: An university student connects 4 ADCs in parallel to increase the resolution of her EE101 lab measurement. She uses a 1:4 clock buffer to distribute the clock to the 4 ADCs. The ADC has a specification for device to device aperture delay variation of ±0.1 ns, while the buffer has a channel to channel skew of 250 ps. Does the skew specification of the buffer meet the ADC aperture delay requirements

Quiz

- True or false: Single ended buffers are immune to external noise coupling
- True or false: For a given VDD and a capacitive load, CMOS buffers provide the highest output amplitude
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