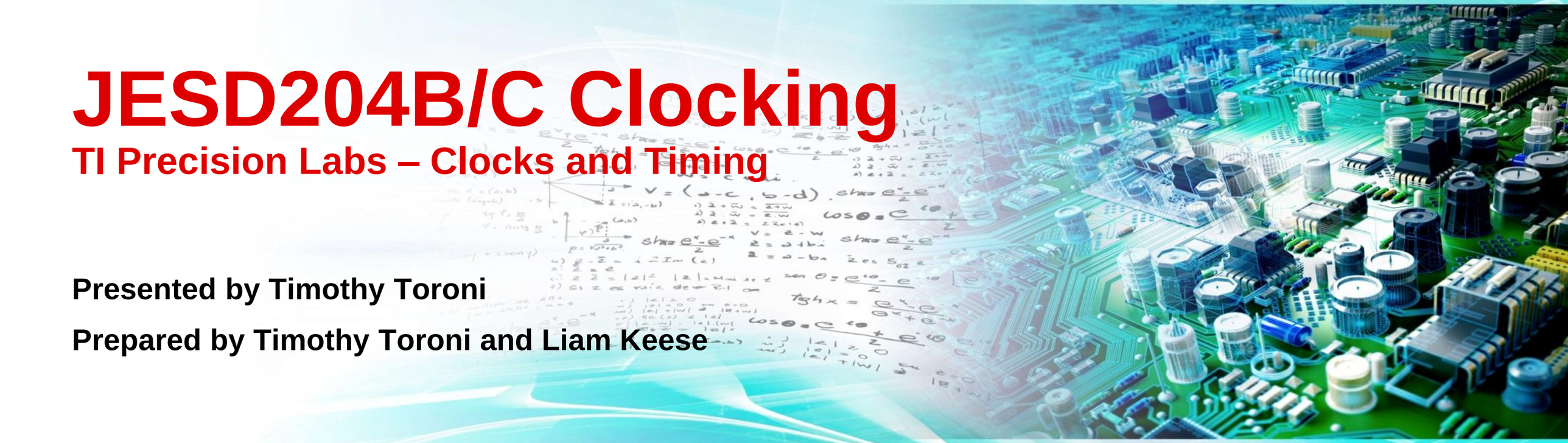
JESD204B/C Clocking

TI Precision Labs – Clocks and Timing

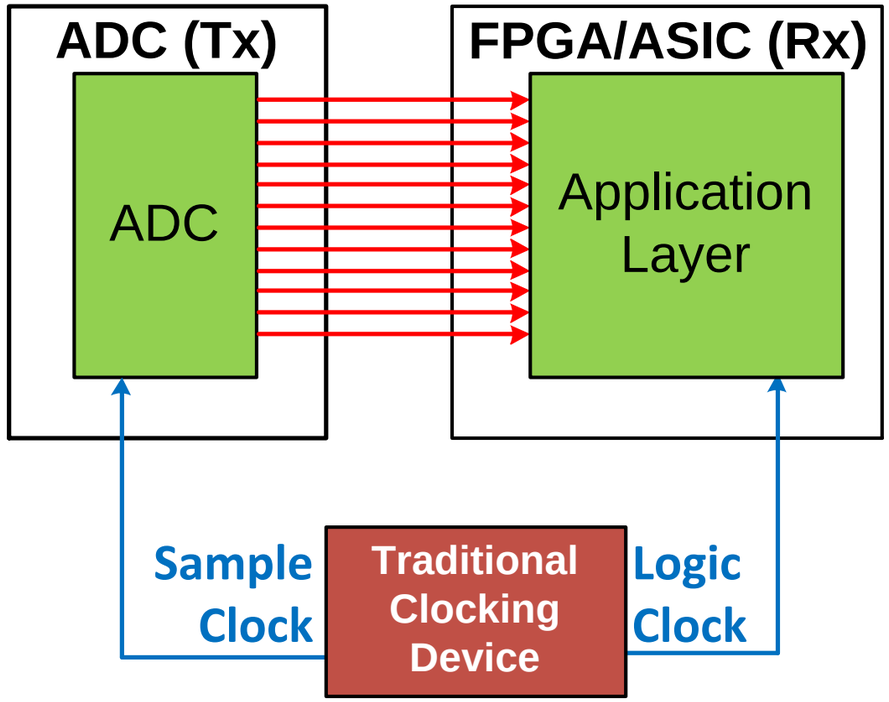


Presented by Timothy Toroni

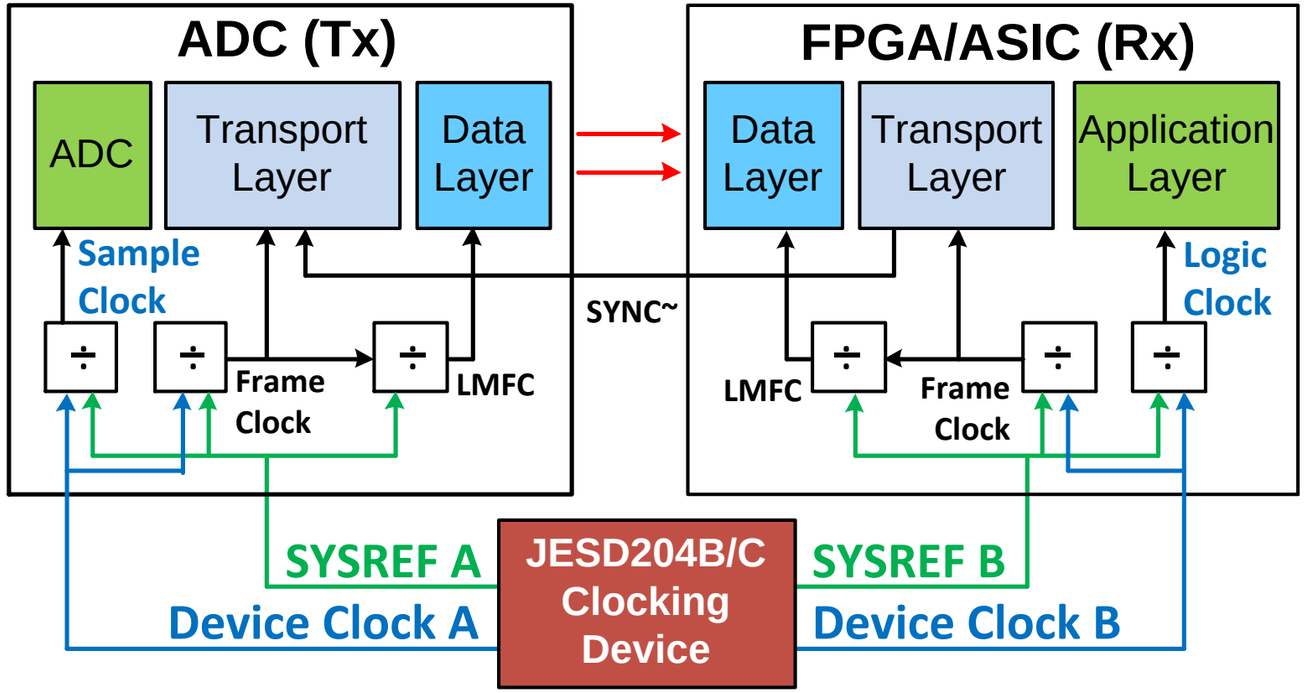
Prepared by Timothy Toroni and Liam Keese

Traditional clocking vs. JESD204B clocking

Traditional clocking with parallel data interface



JESD204B clocking and data interface



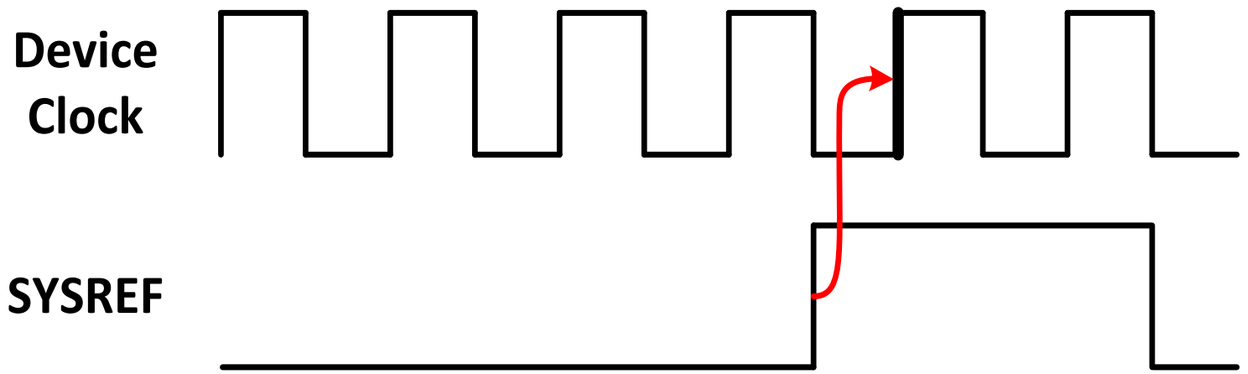
What is JESD204?

- JESD204 is a definition for data converters to allow **synchronization of data** between **data converters** and **logic devices**.

Function	JESD204	JESD204A	JESD204B	JESD204C
JEDEC specification release	2006	2008	**2011**	**2017**
Maximum lane rate (Gbps)	3.125	3.125	**12.5**	**32**
Support for multiple lanes?	No	Yes	**Yes**	**Yes**
Support for lane synchronization?	No	Yes	**Yes**	**Yes**
Support for multi-device synchronization?	No	Yes	**Yes**	**Yes**
Support for deterministic latency?	No	No	**Yes**	**Yes**
Support for harmonic clocking?	No	No	**Yes**	**Yes**

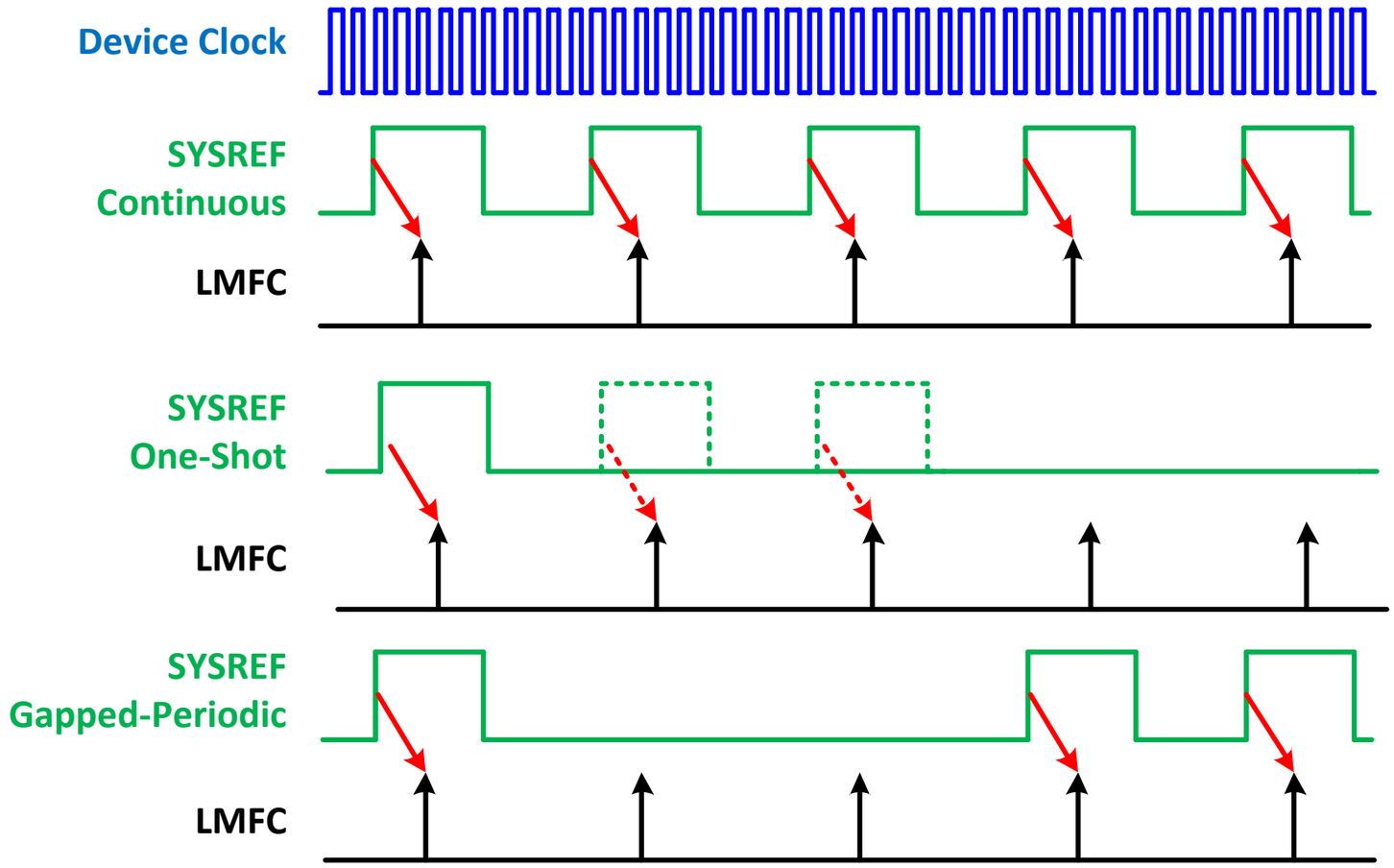
JESD204B subclasses

- Subclass 0
  - No support for deterministic latency (backward compatible with JESD204A)
- Subclass 2
  - Deterministic latency achieved using “~SYNC“ as timing signal
- Subclass 1
  - Deterministic latency achieved using an external “SYSREF” as timing signal



Types of SYSREF signals

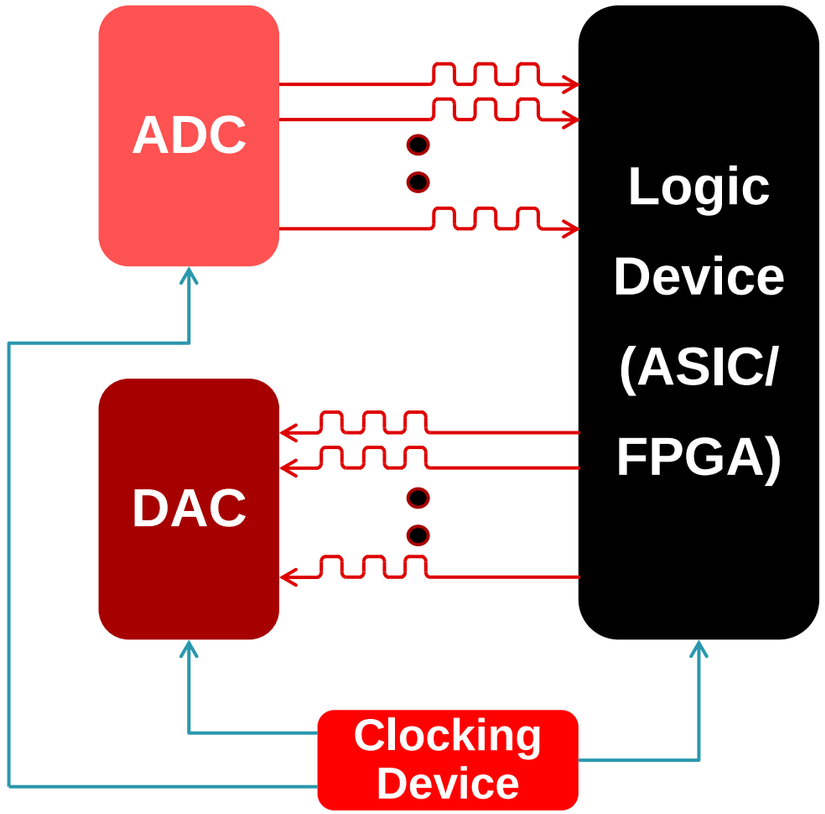
- Continuous SYSREF
- One-shot SYSREF
  - Single (or multiple) pulses only when requested
  - Reduces radiated spurious noise
- Gapped Periodic SYSREF
  - Reduces radiated spurious noise



Benefits of JESD204B – Reduced PCB complexity

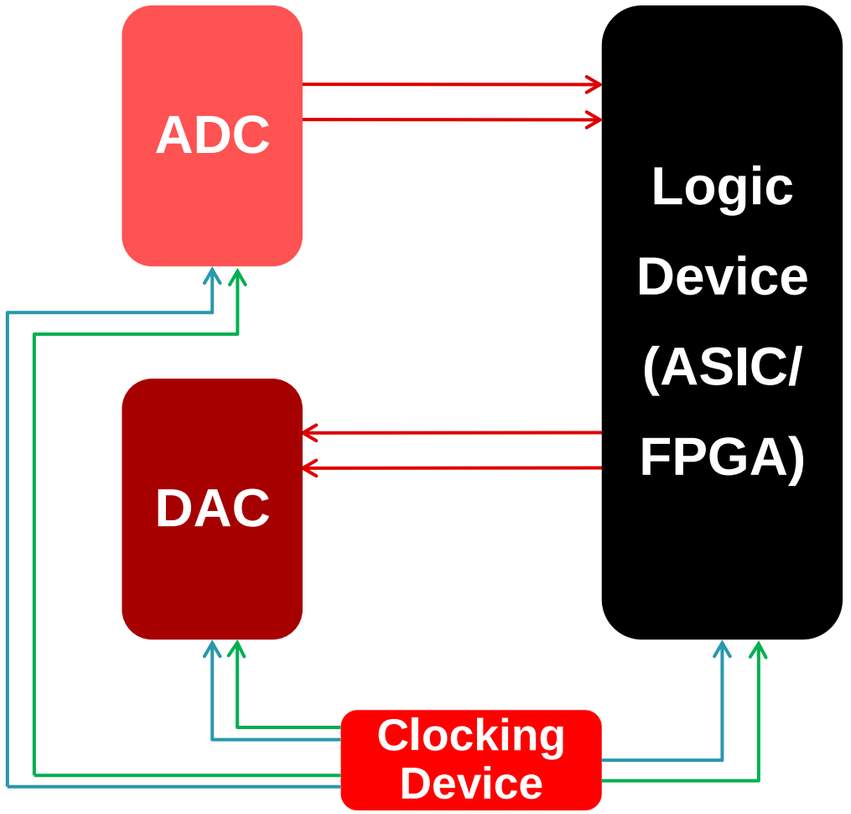
Traditional clocking with parallel data interface

Many low speed parallel lanes with length matching



JESD204B clocking and data interface

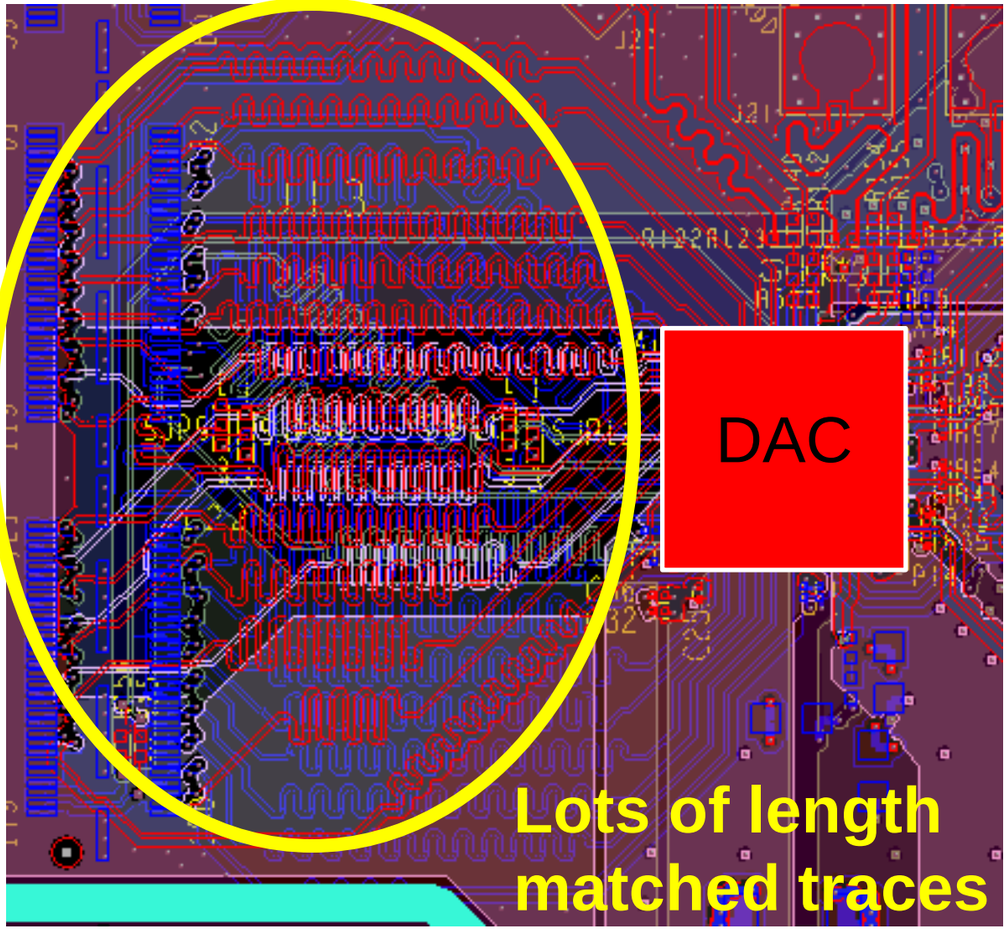
Single or few serialized high speed lanes without the need for length matching



Example of non-JESD204B vs. JESD204B layout

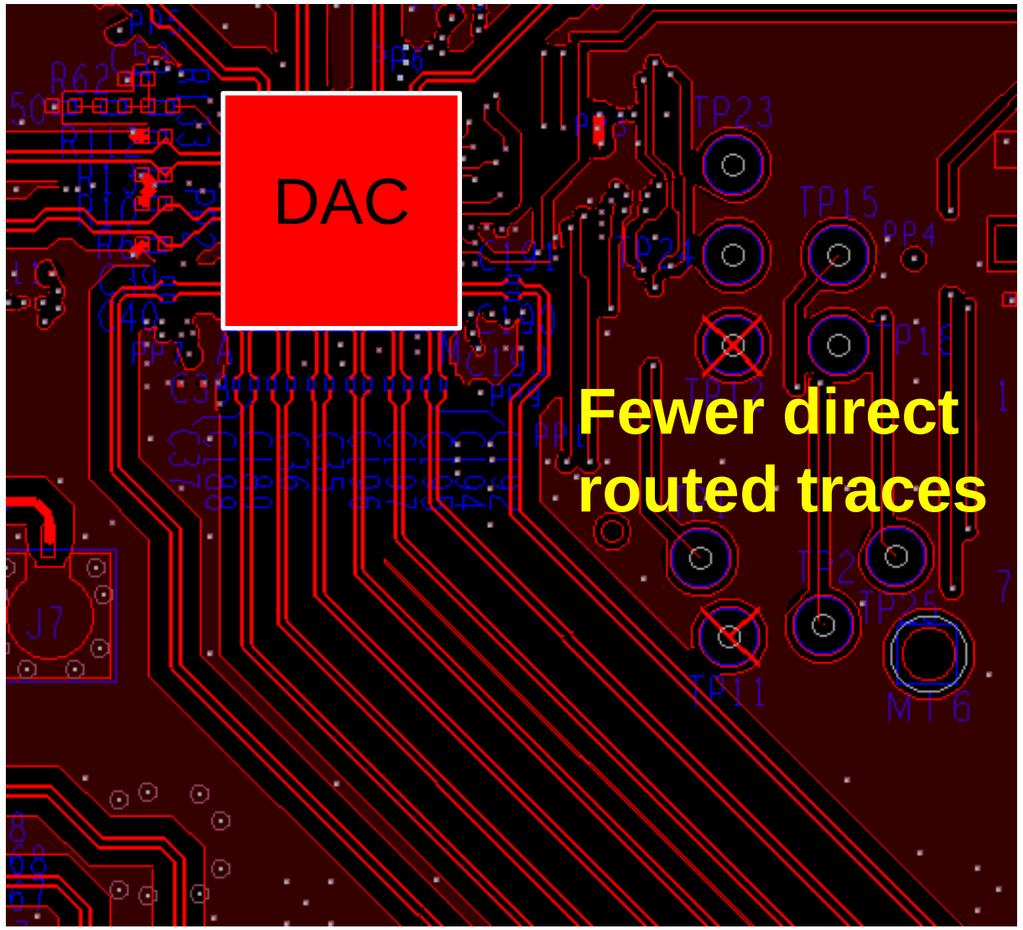
Non-JESD204B DAC (LVDS)

32 lanes, 750 MSPS



JESD204B DAC (JESD204B)

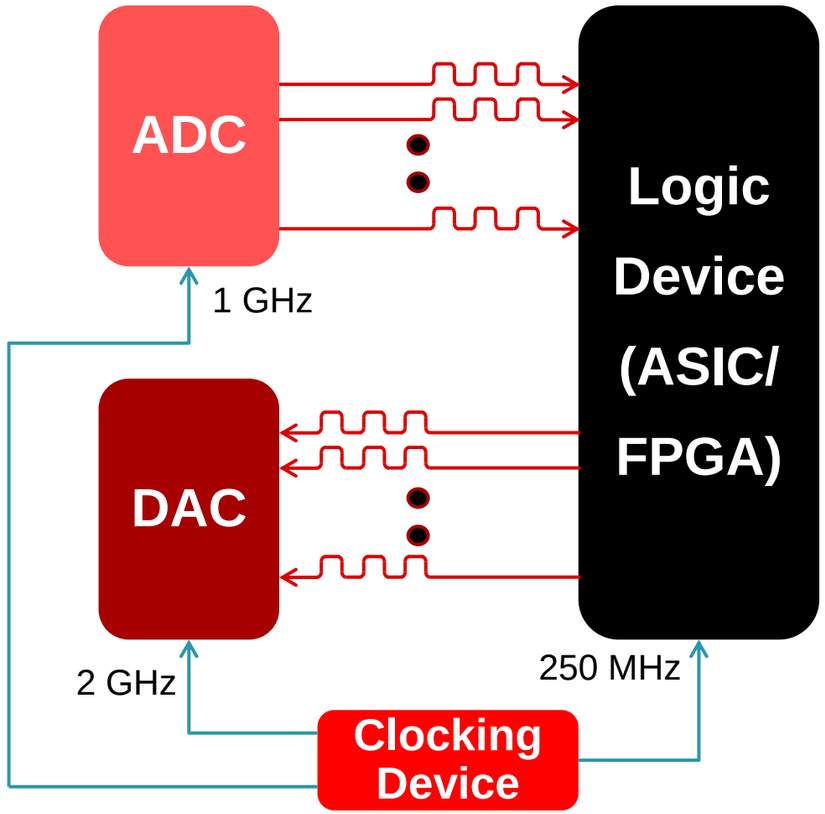
8 lanes, 1250 MSPS



Benefits of JESD204B – Reduced clock frequencies

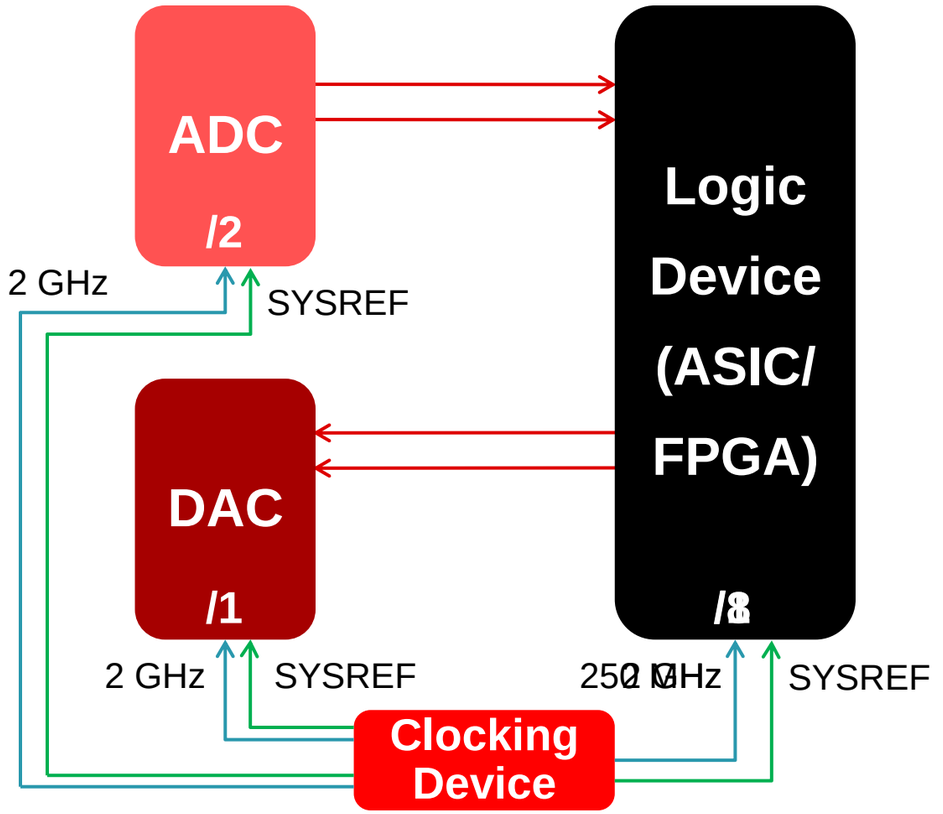
Traditional clocking with parallel data interface

Different clock frequencies
for each device



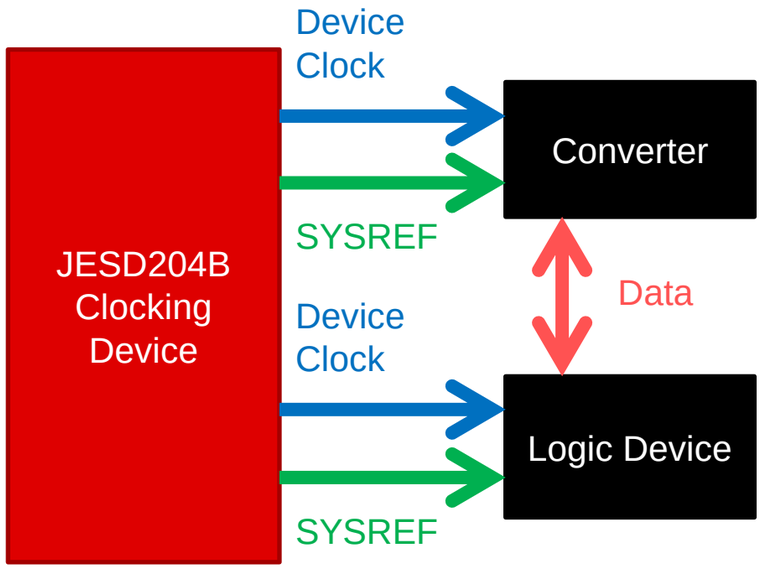
JESD204B clocking and data interface

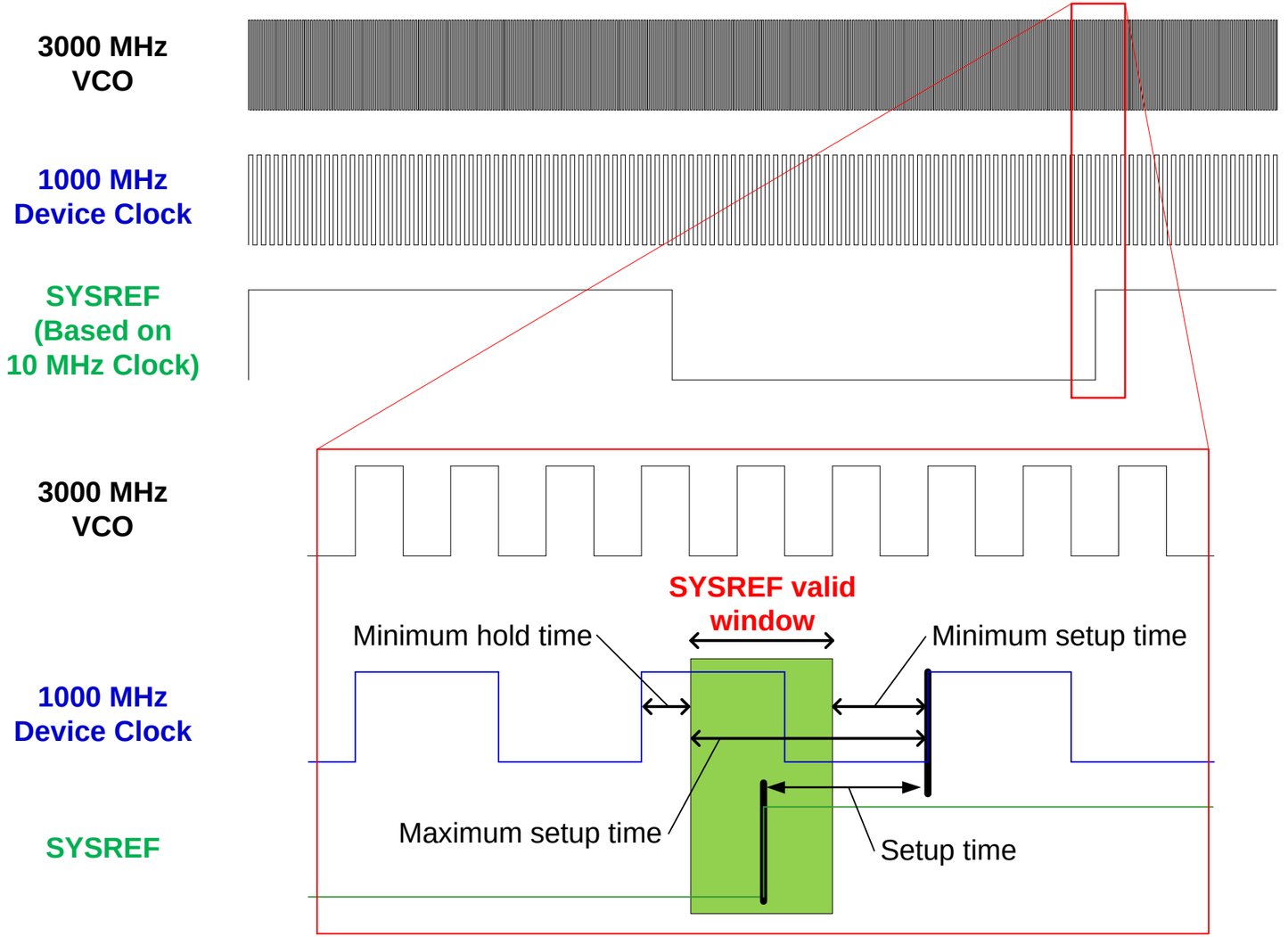
Single clock frequency
for each device, with exception



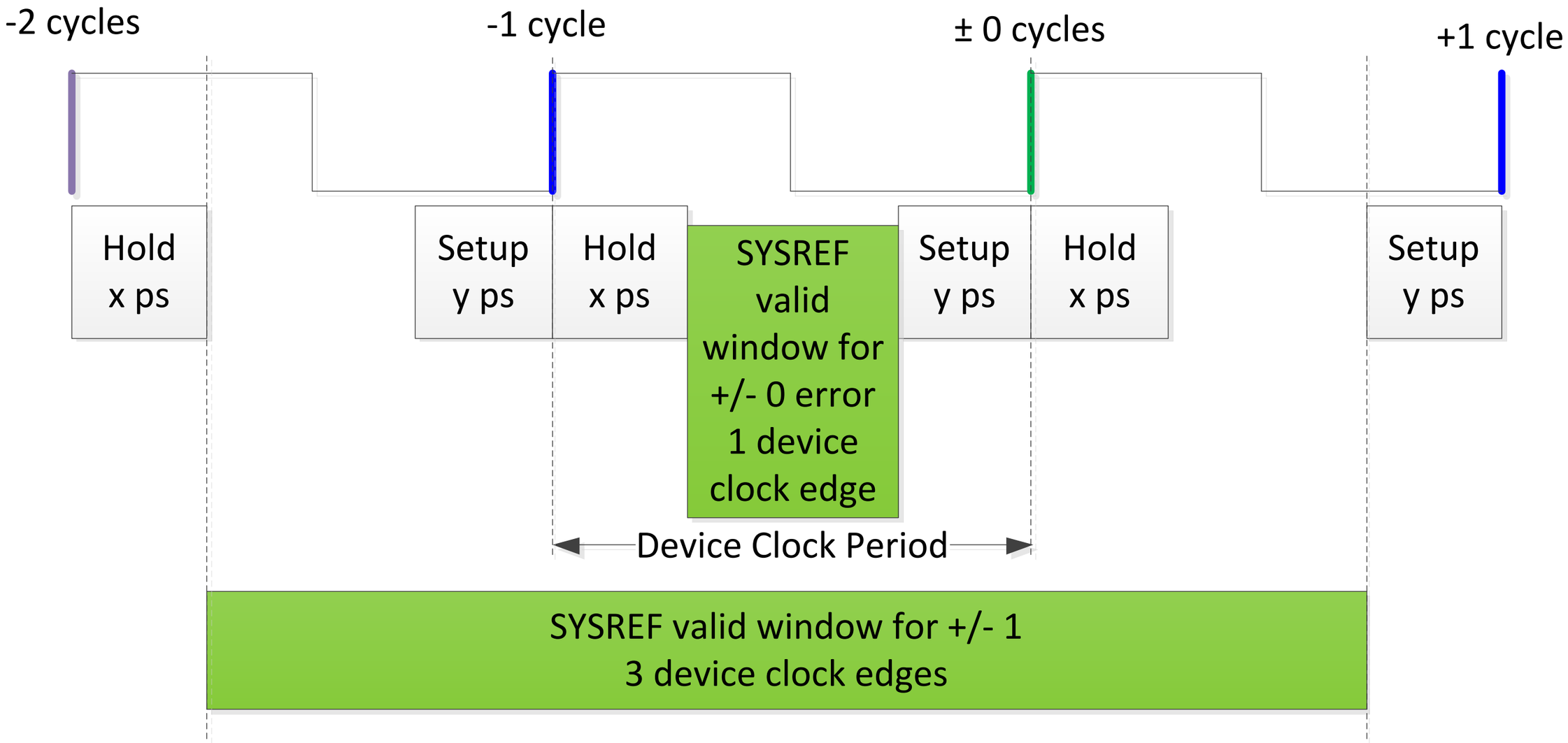
JESD204B subclass 1: determinism with SYSREF

- Deterministic timing/data transfer achieved by repeatable “marking” of device clocks across system elements.



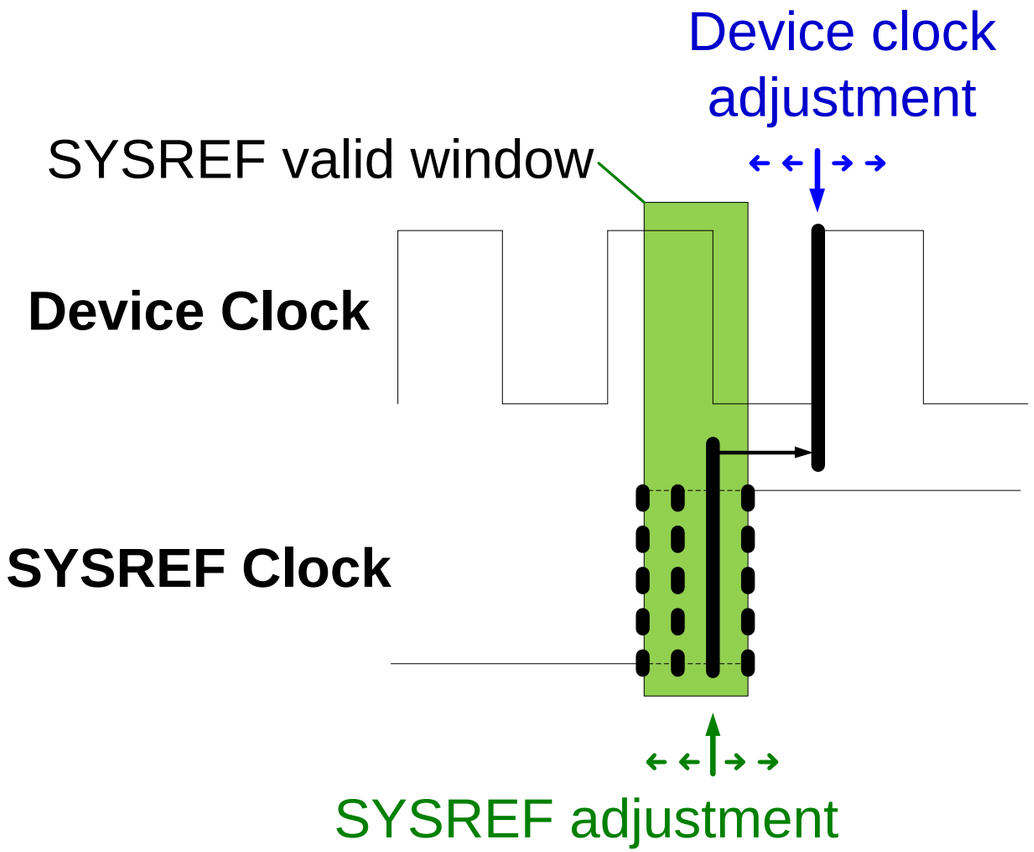


What if timing is missed?



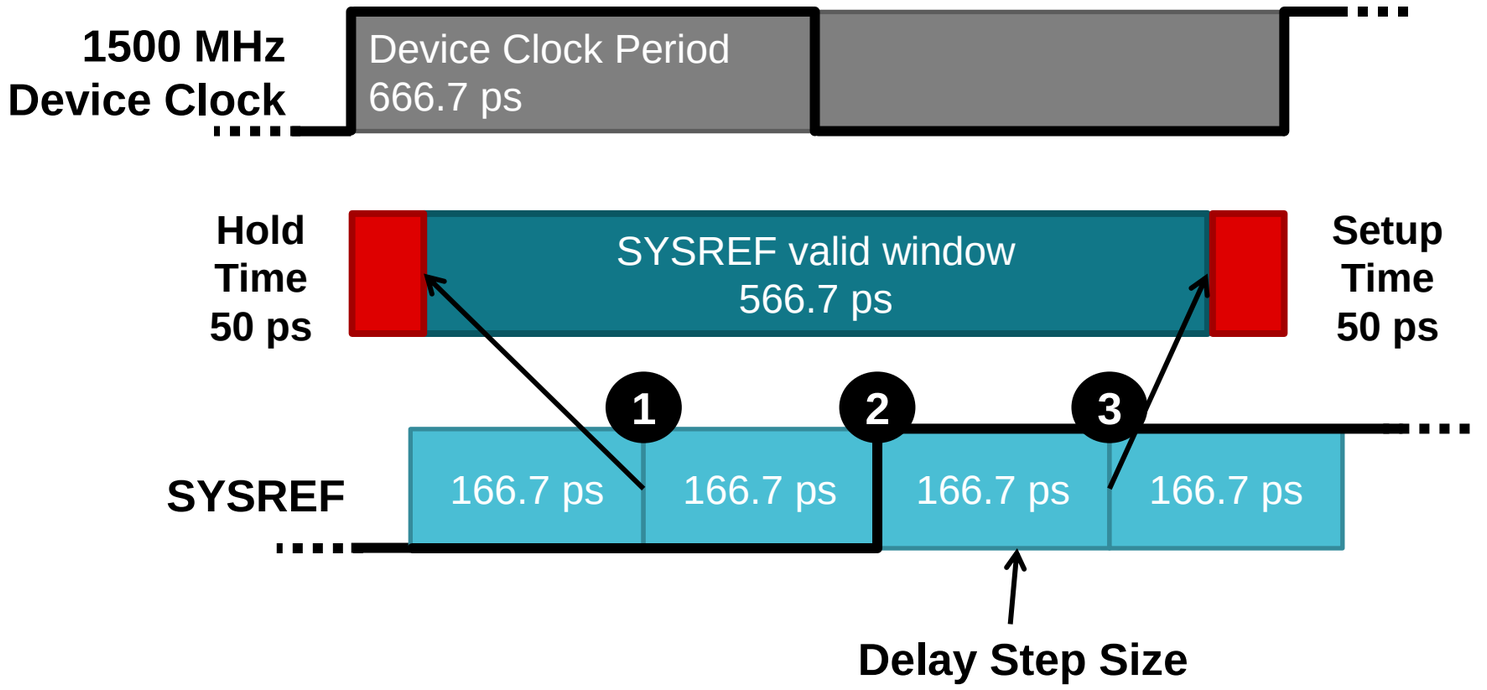
Device clock and SYSREF timing adjustment

- Device clock
  - Adjusted to minimize skew between device clocks
- SYSREF
  - Adjusted to optimize timing to SYSREF valid window.
- Delay adjustment types:
  - Digital delay
  - Analog delay



SYSREF example 1:
SYSREF valid window greater than three times delay step

- 3000 MHz VCO frequency
- 1500 MHz device clock, 666.7 ps period
- 50 ps setup/hold time
- Valid window = 566.7 ps



Equations:

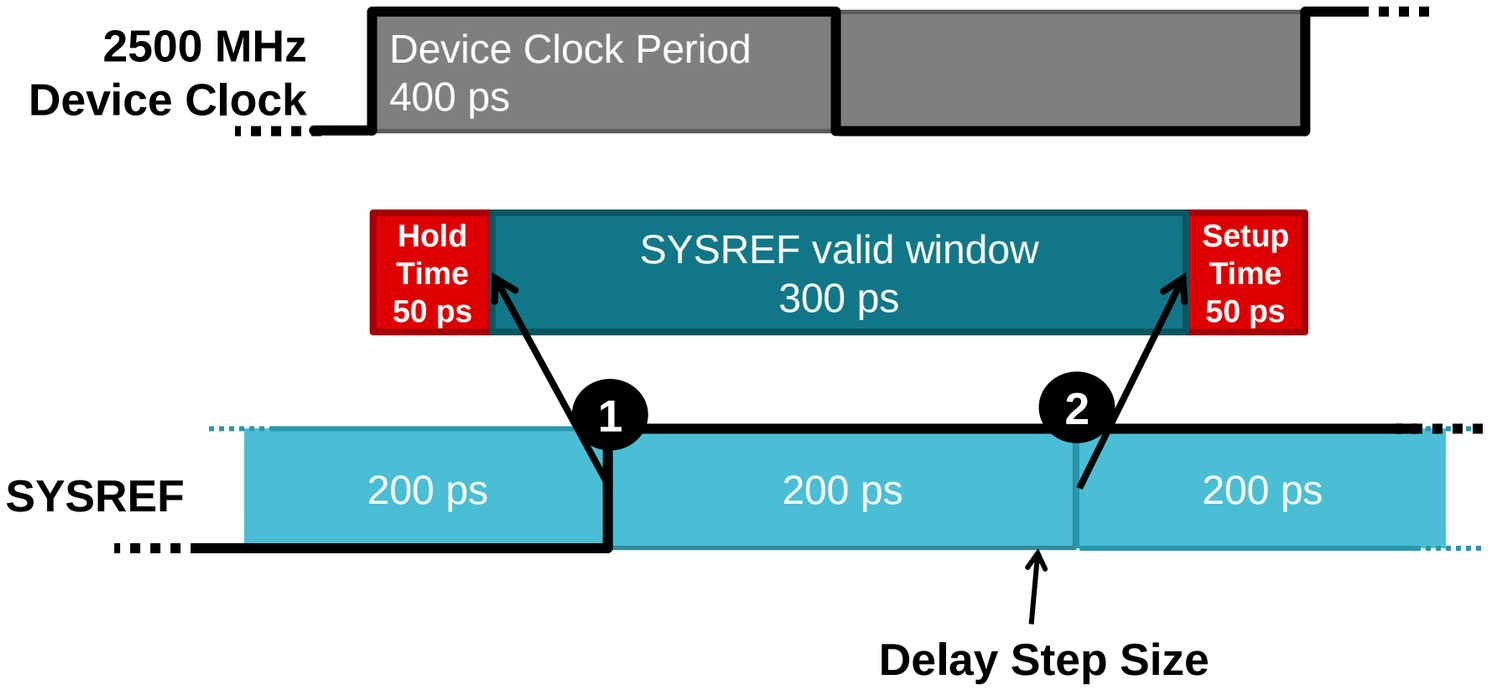
Valid window = device clock period – setup time – hold time

$$Margin = min(Delay\ Step\ Size);\ if\ 3 * \max(Delay\ Step\ Size) < SYSREF\ valid\ window$$

Min and max delay step size is to account for possible non-uniform step sizes.

SYSREF example 2:
SYSREF valid window less than three times delay step

- 2500 MHz VCO
- 2500 MHz device clock, 400 ps period
- 50 ps setup/hold time
- Valid window = 300 ps



Equations:

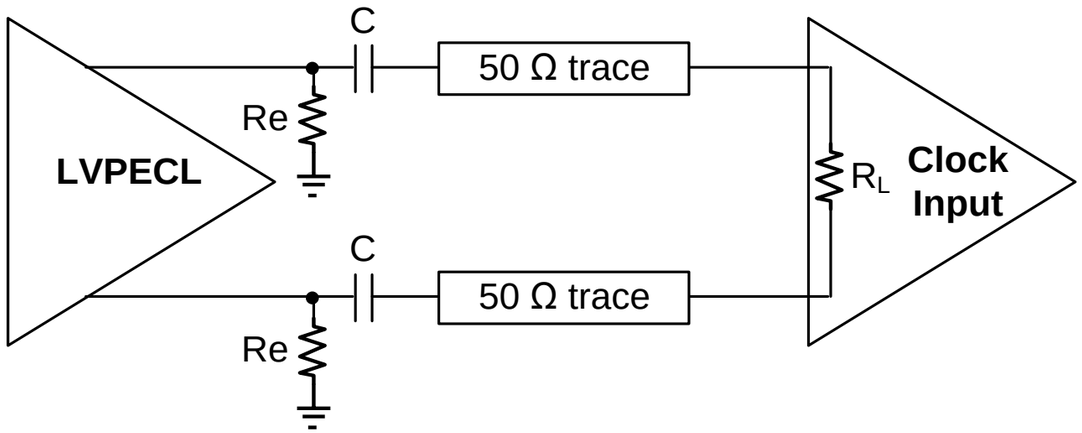
Valid window = device clock period – setup time – hold time

$$Margin = \frac{Valid\ Window\ - max(Delay\ Step\ Size)}{2}$$

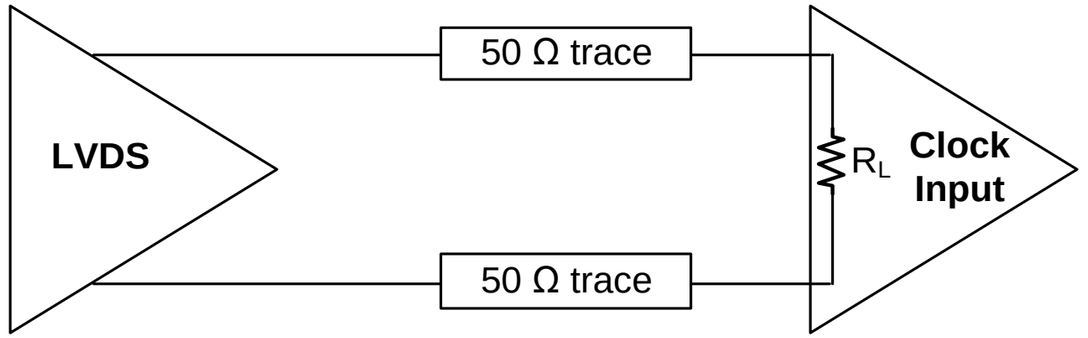
Min and max delay step size is to account for possible non-uniform step sizes.

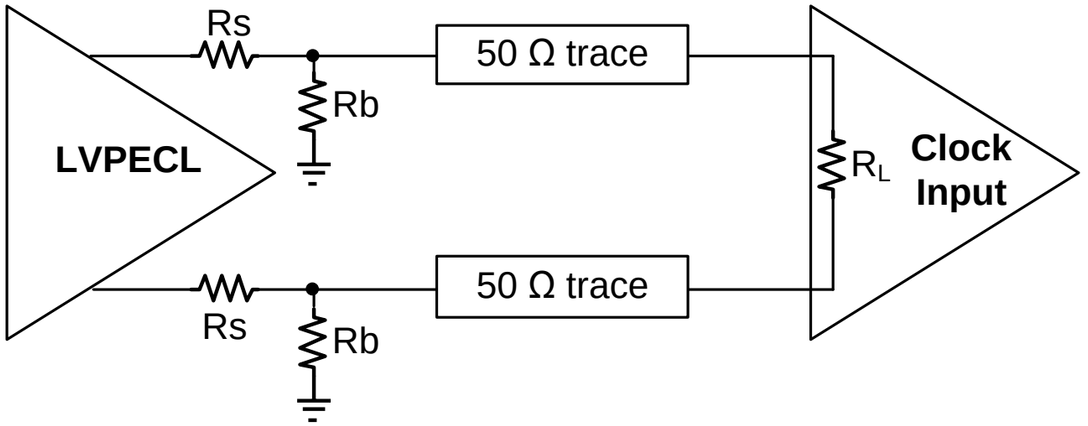
Interface between clock and target

AC Coupled Clock



DC Coupled Clock





To find more clocks and timing technical resources and search products, visit ti.com/clocks

Quiz

1. True or false: SYSREF is used to synchronize a JESD204B system when using subclass 1?
2. True or false: JESD204B simplifies PCB design for data traces?
3. True or false: The SYSREF valid window is the time in which a rising SYSREF edge must occur to deterministically mark a device clock as a time reference point?
4. True or false: AC coupling clocks simplifies the interface as common mode voltage is of no concern?
5. True or false: DC coupling the SYSREF simplifies synchronization of the JESD204B system?

Quiz: Answers

1. True or false: SYSREF is used to synchronize a JESD204B system when using subclass 1?
2. True or false: JESD204B simplifies PCB design for data traces?
3. True or false: The SYSREF valid window is the time in which a rising SYSREF edge must occur to deterministically mark a device clock as a time reference point?
4. True or false: AC coupling clocks simplifies the interface as common mode voltage is of no concern?
5. True or false: DC coupling the SYSREF simplifies synchronization of the JESD204B system?