PLL Transient Response

TI Precision Labs – Clocks and Timing

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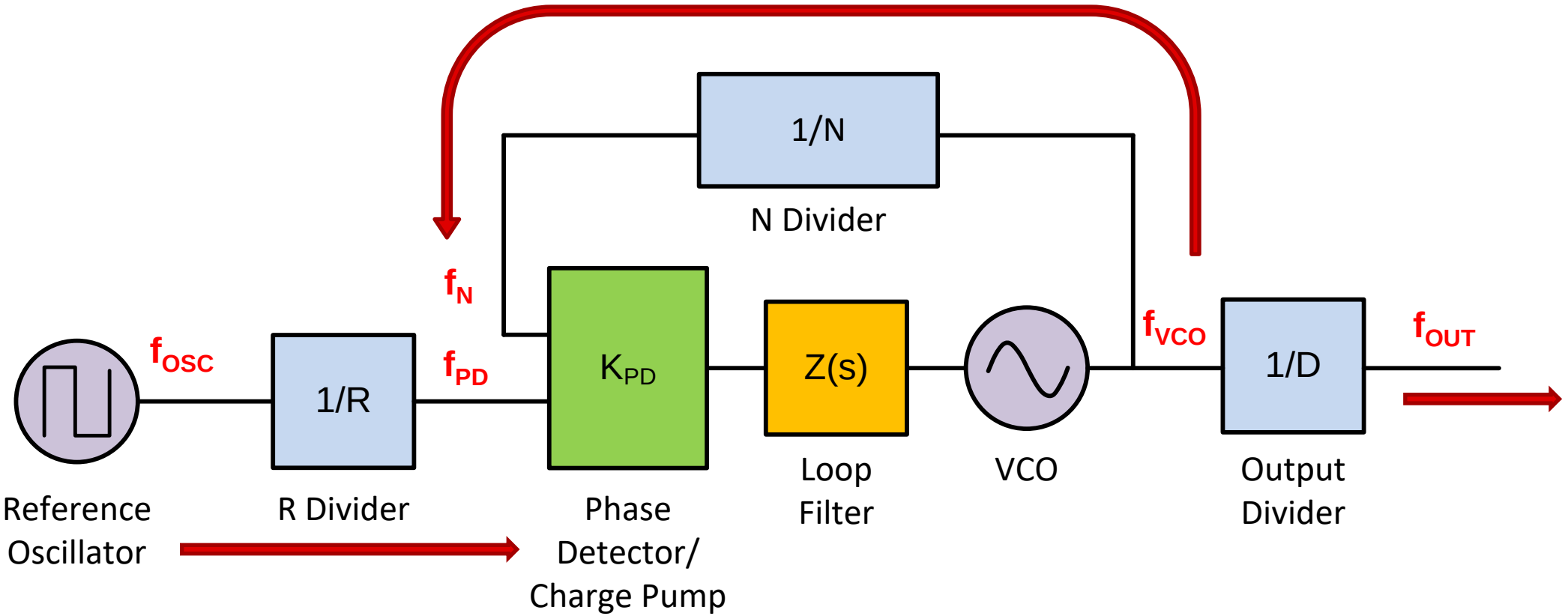
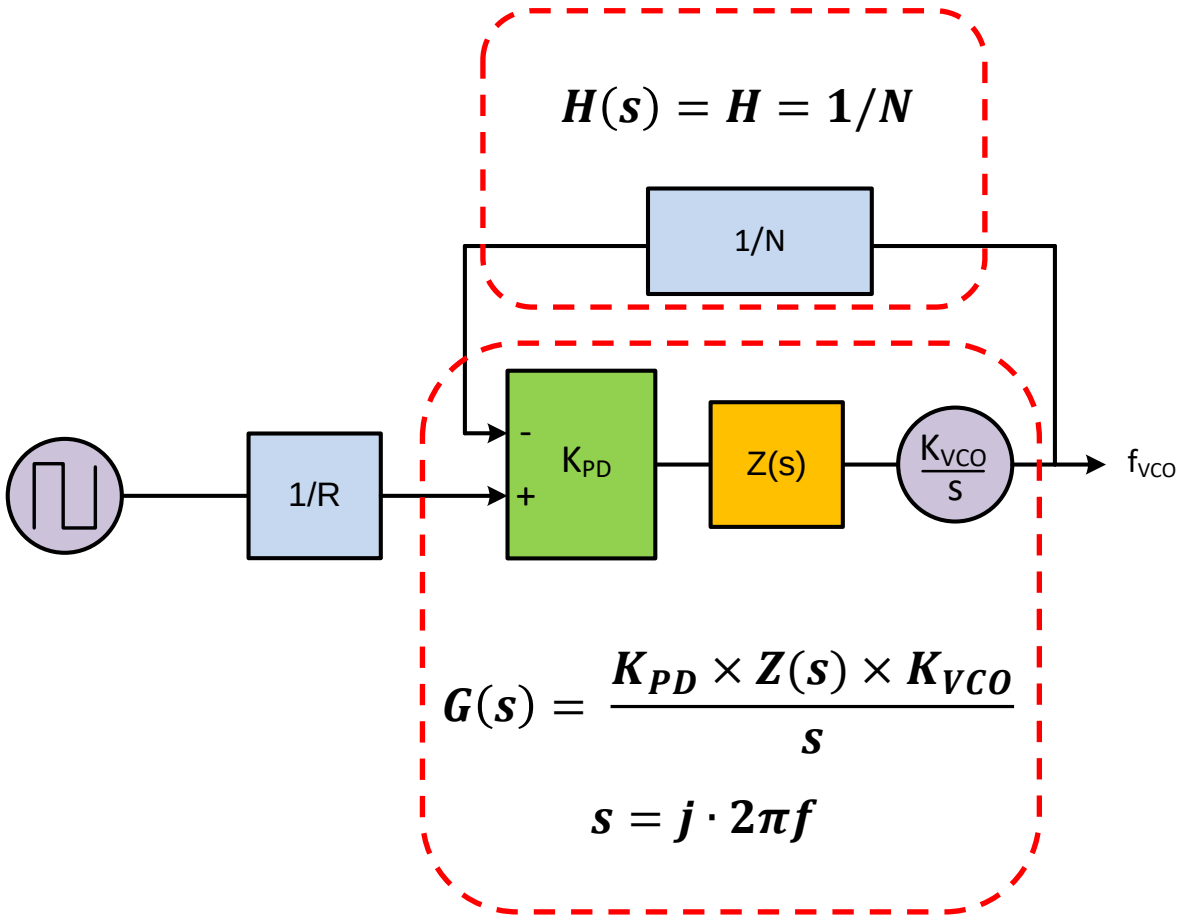
Phase lock loop overview



PLL loop bandwidth (BW)

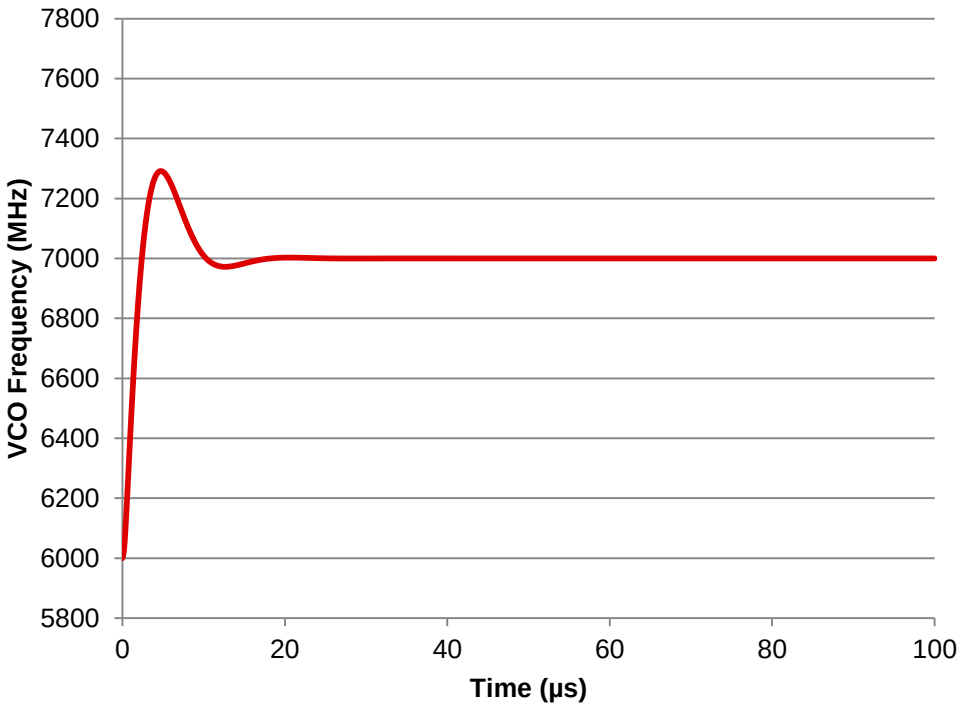


Block	Transfer Function
OSC	$\frac{1}{R} \cdot \frac{G(s)}{1 + G(s) \cdot H}$
R/N Dividers	$\frac{G(s)}{1 + G(s) \cdot H}$
Phase Detector	$\frac{1}{K_{PD}} \cdot \frac{G(s)}{1 + G(s) \cdot H}$
VCO	$\frac{1}{1 + G(s) \cdot H}$

$$BW \equiv f : |G(s) \times H| = 1$$

PLL transient response overview

Analog loop filter transient

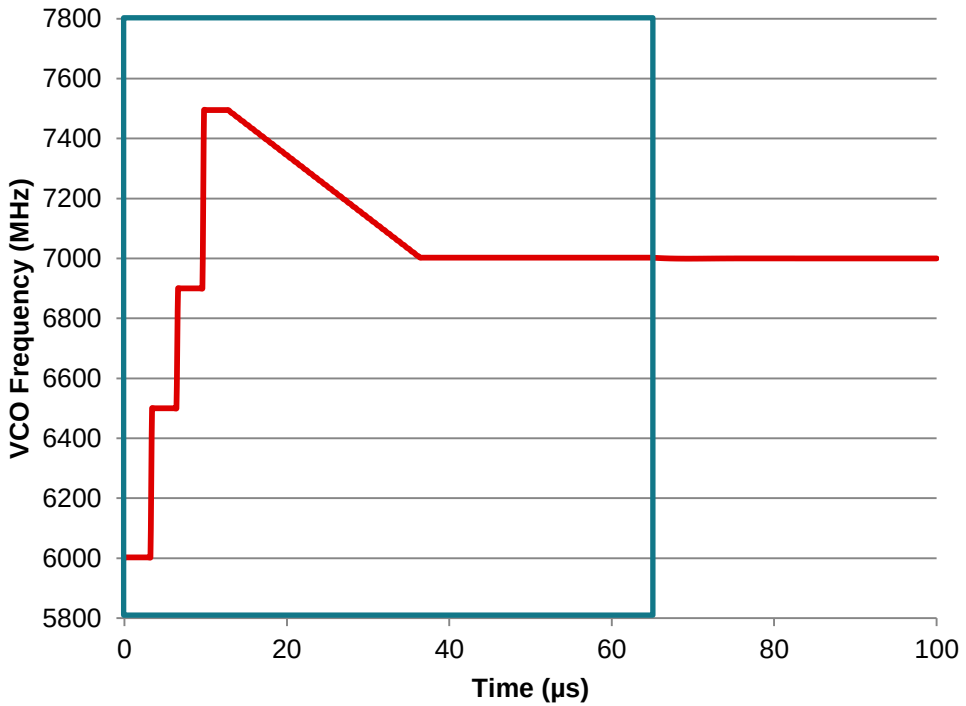


Analog lock time = 48 µs

Total lock time = 48 µs

PLL transient response overview

Transient with VCO calibration



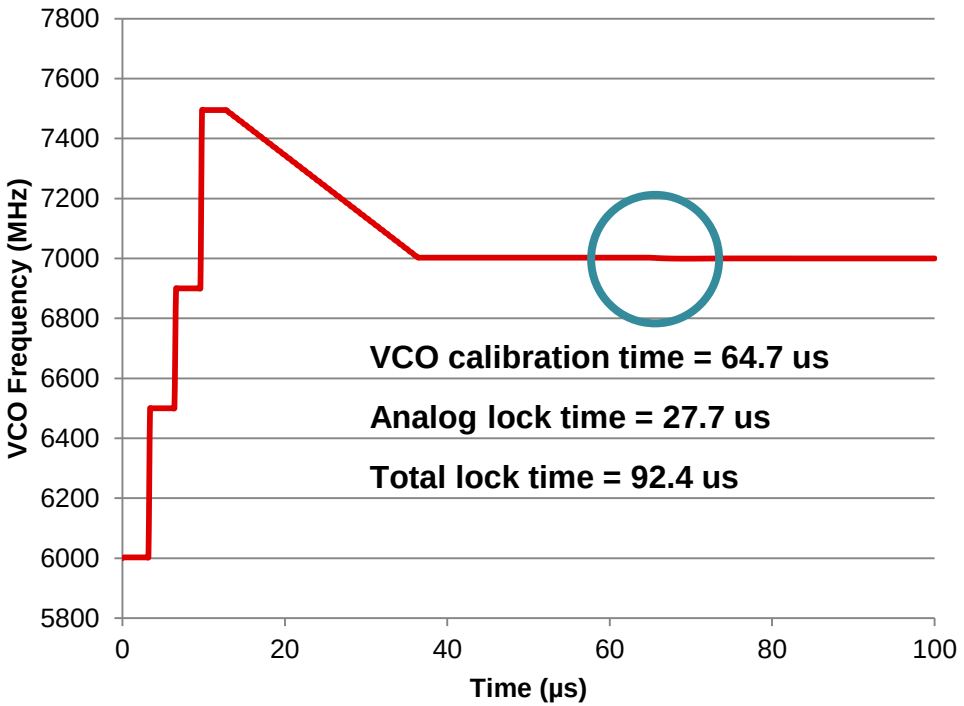
VCO calibration time = 64.7 us

Analog lock time = 27.7 us

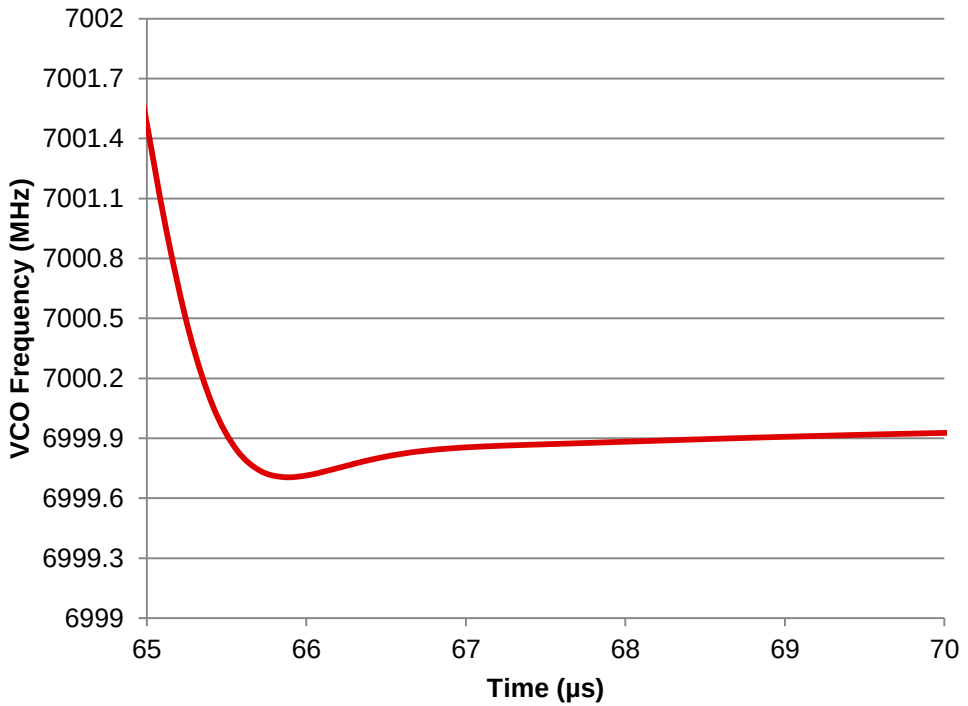
Total lock time = 92.4 us

PLL transient response overview

Transient with VCO calibration

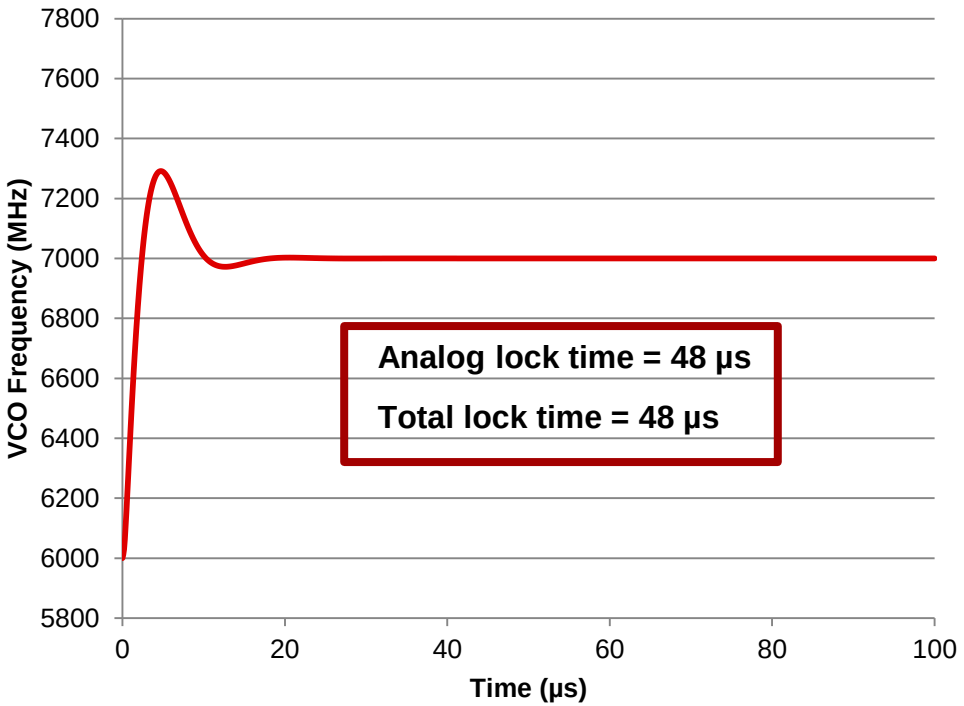


Zoomed in with VCO calibration

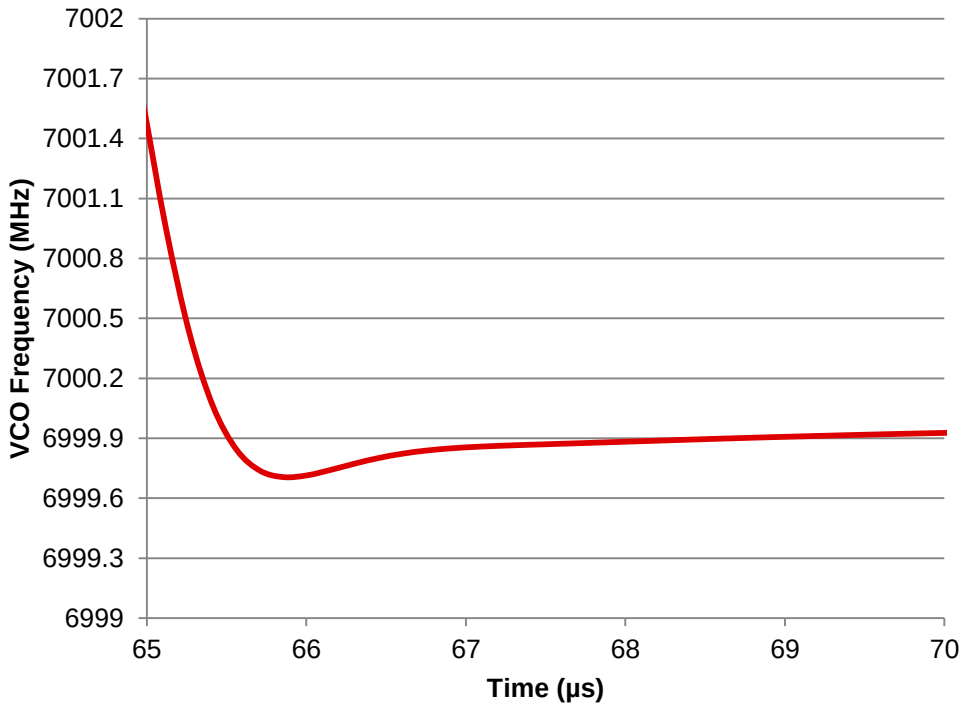


PLL transient response overview

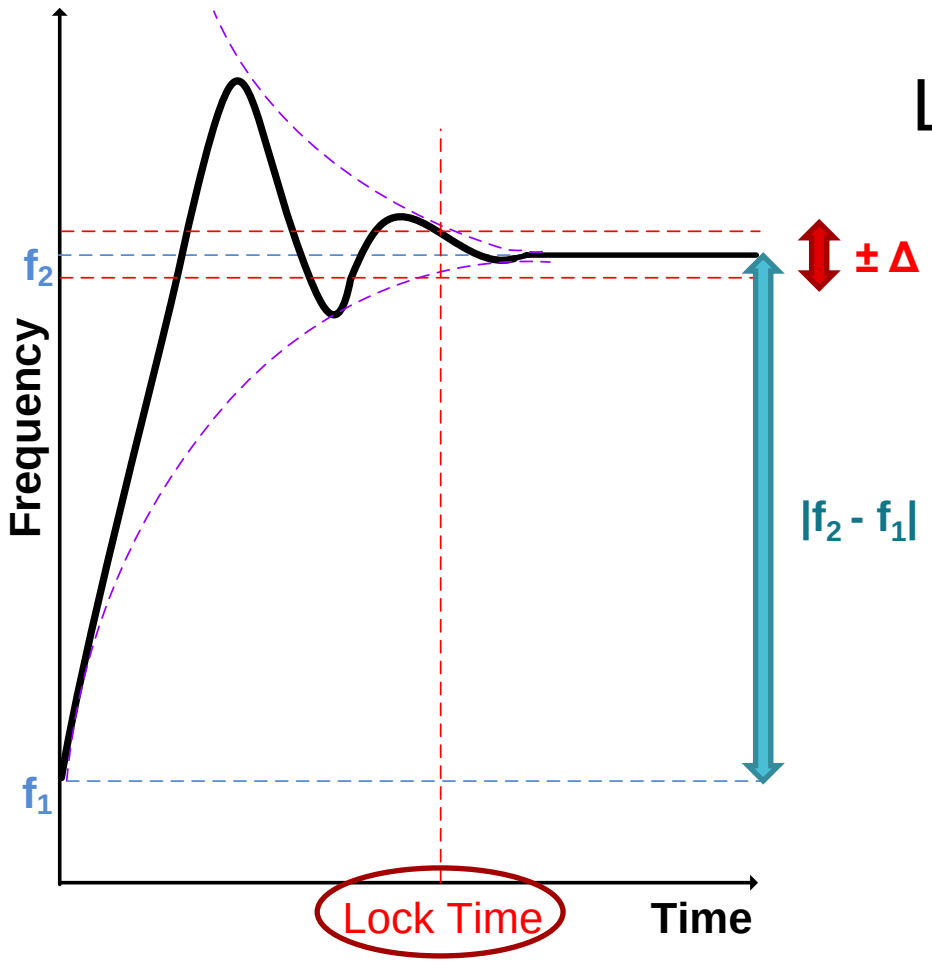
Analog loop filter transient



Zoomed in with VCO calibration



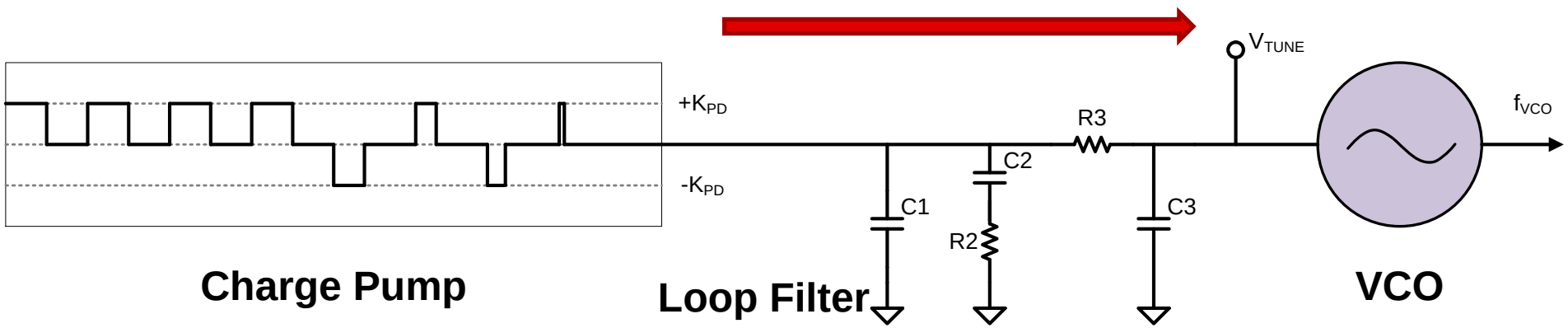
Lock time



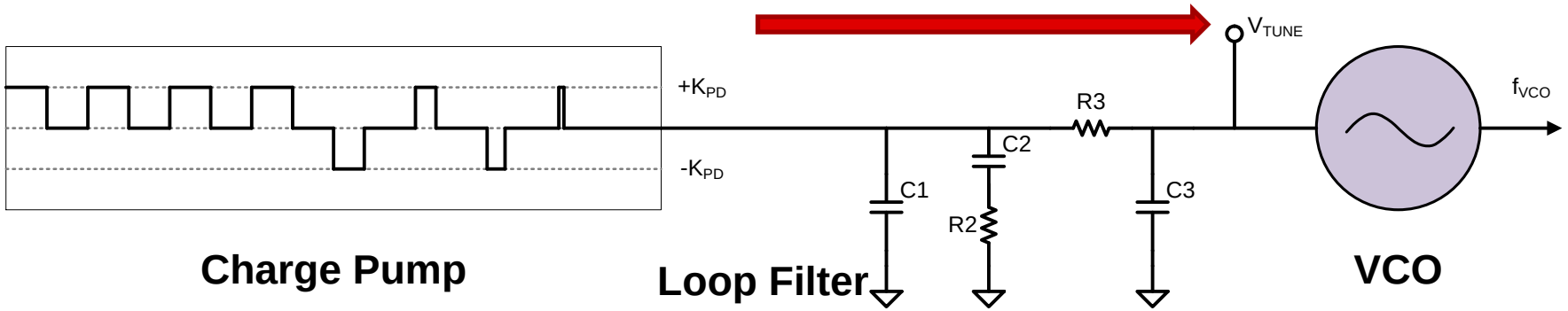
Lock time depends on:

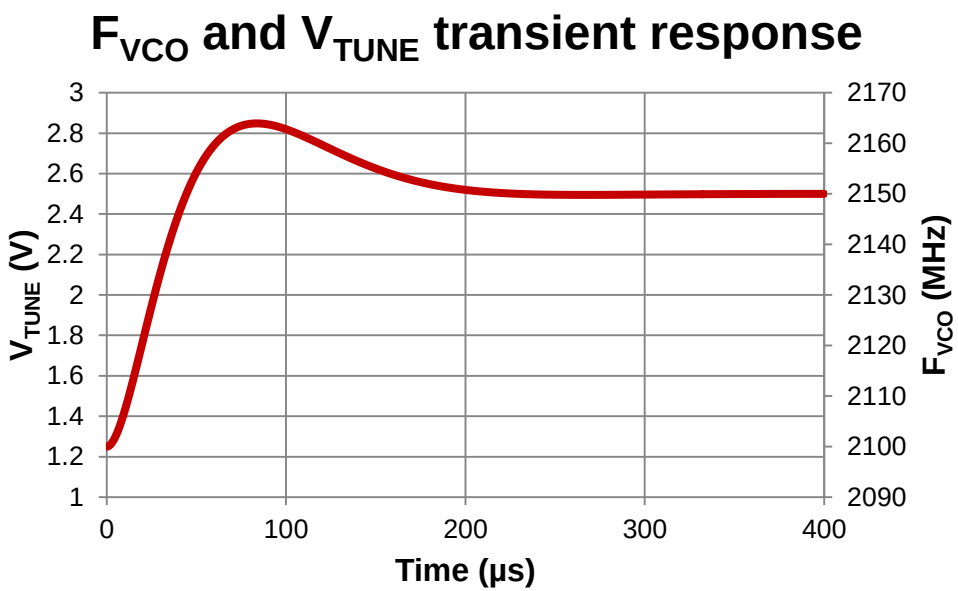
- Frequency jump $|f_2 – f_1|$
- Tolerance (Δ)
- Loop Bandwidth (BW)
- PLL Phase Margin (PM)

Transient response

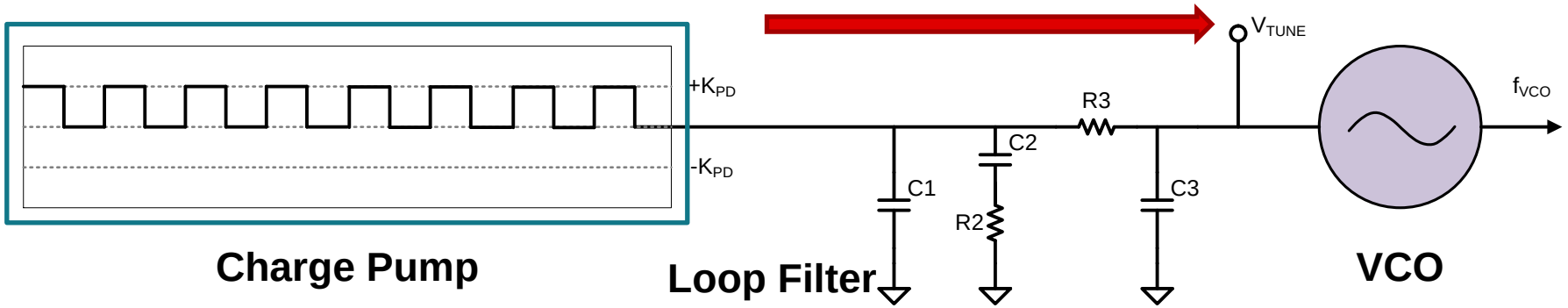


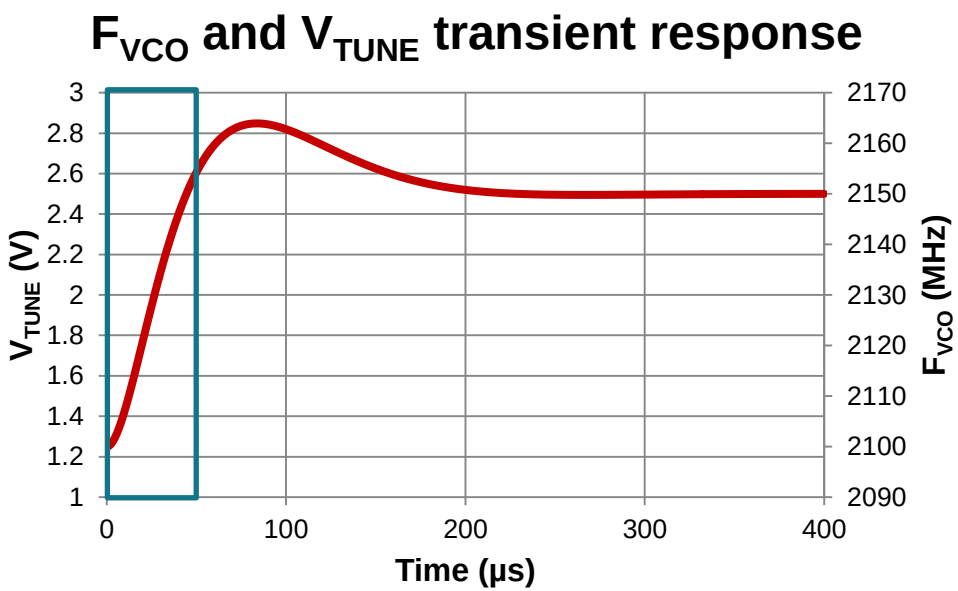
Transient response



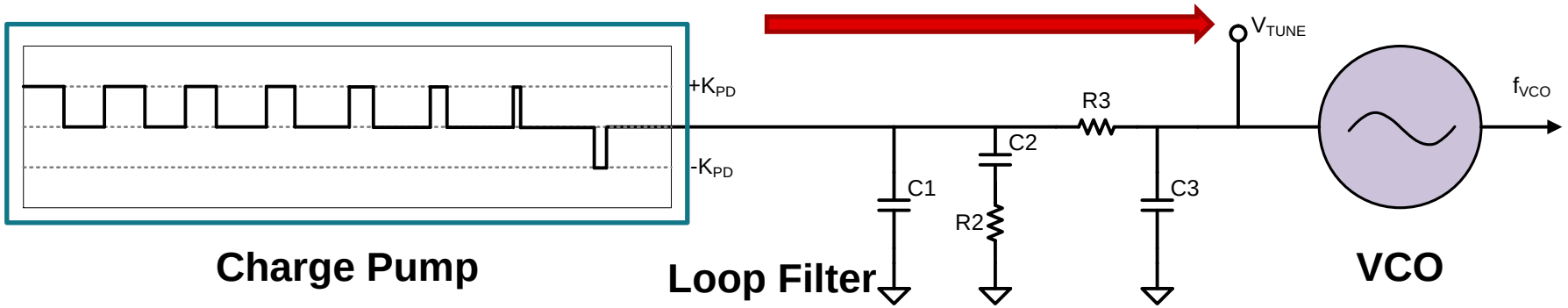


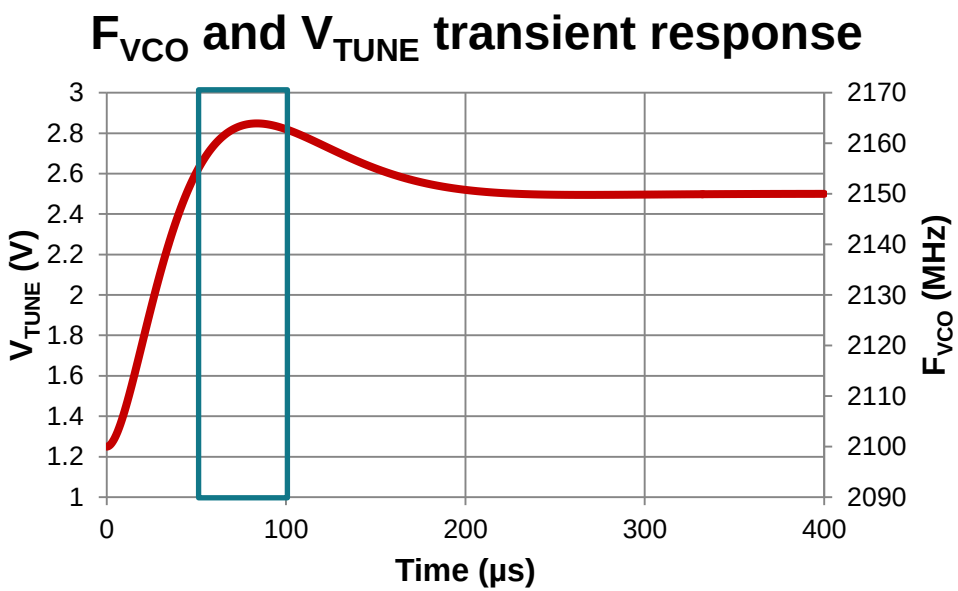
Transient response



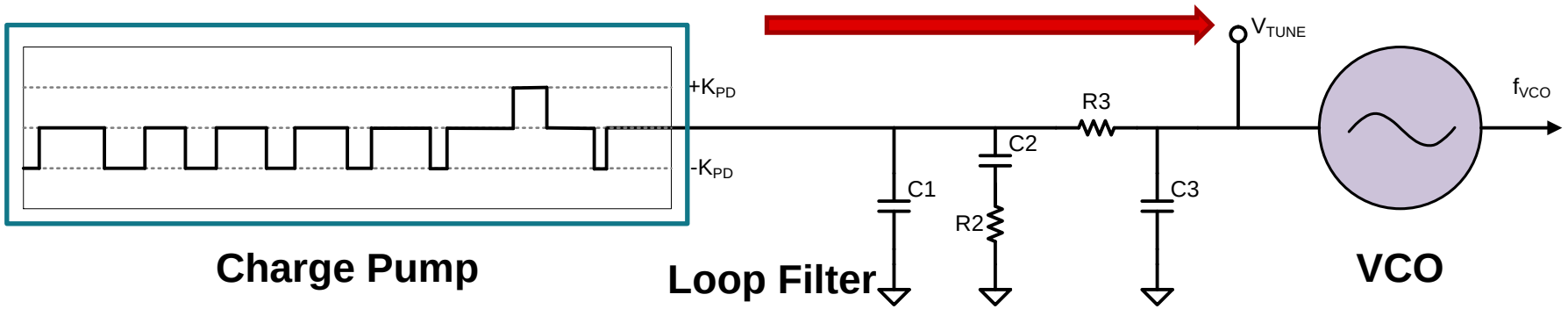


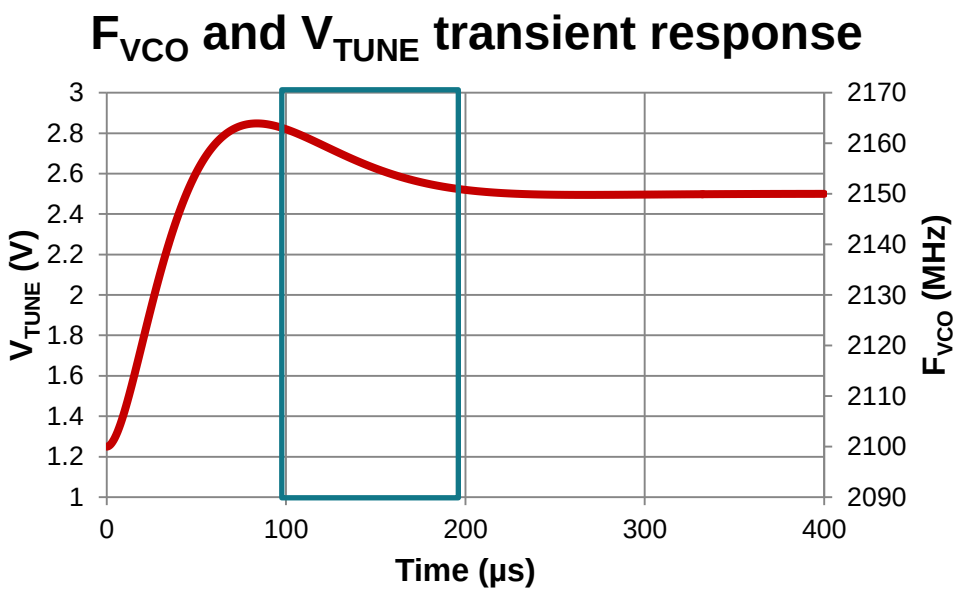
Transient response



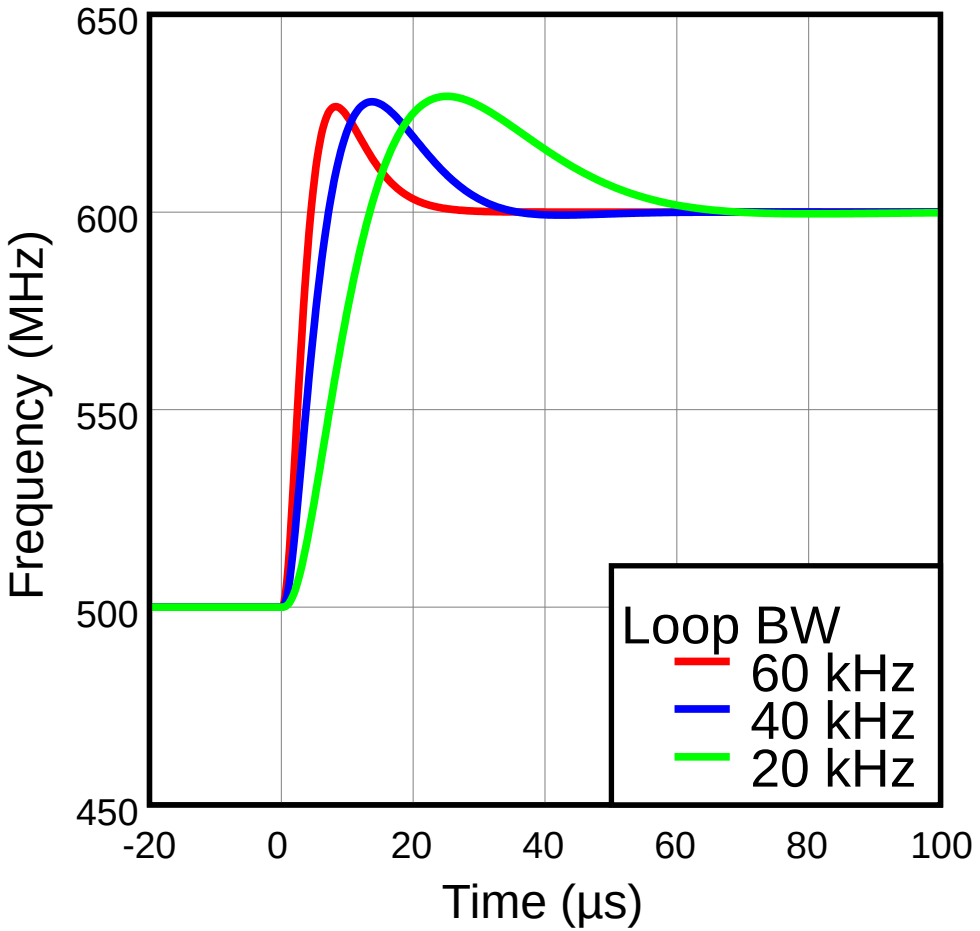


Transient response





Bandwidth's impact on lock time

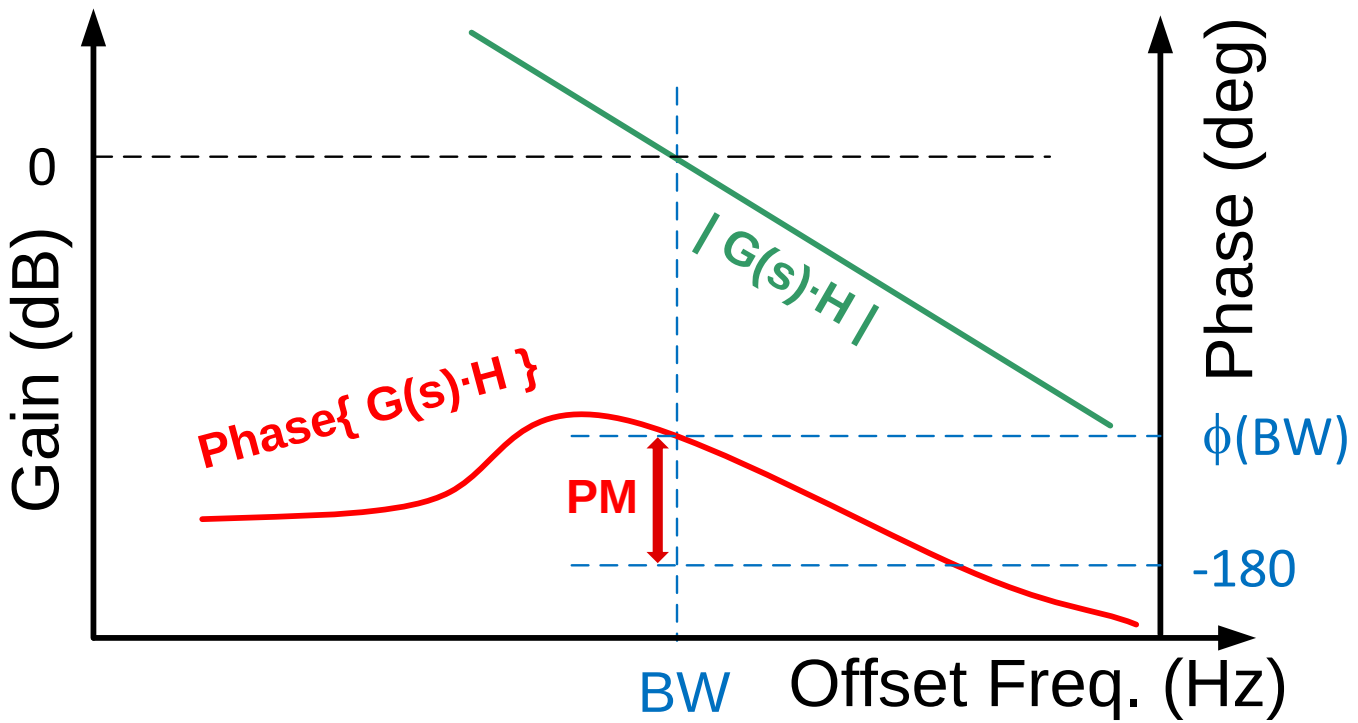


$$BW \equiv f : |G(s) \times H| = 1$$

$$T_{lock} \cong \frac{4}{BW}$$

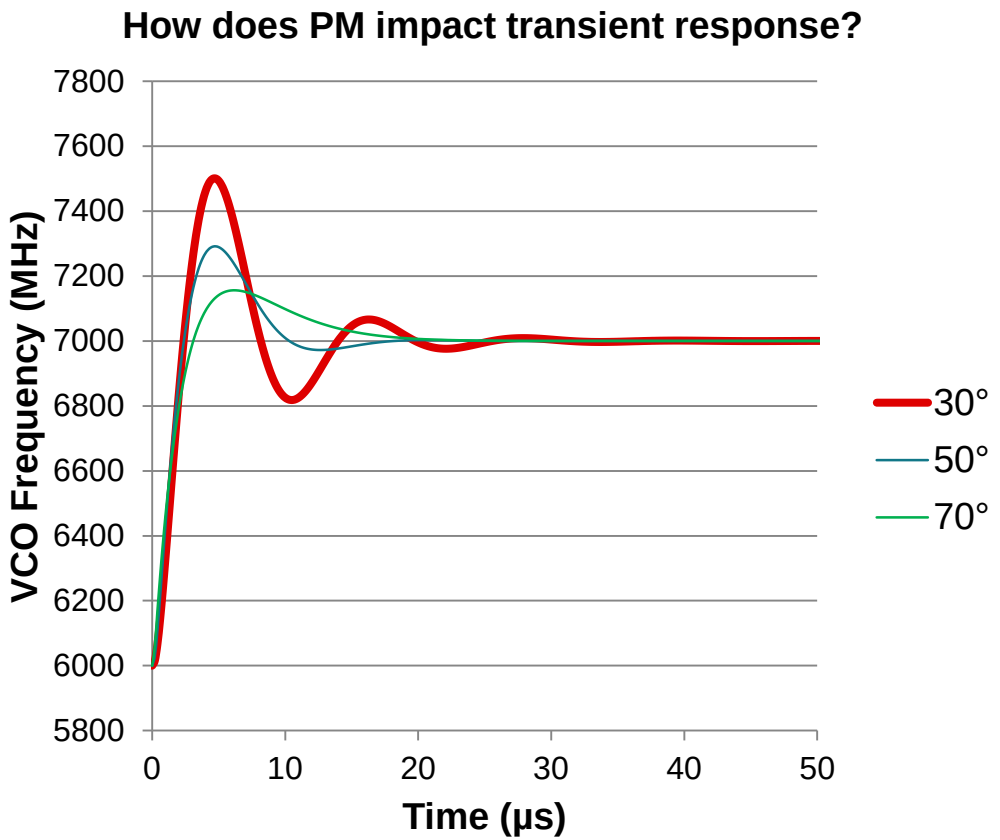
- Wide loop bandwidth reduces lock time
- Narrow loop bandwidth increase lock time

Phase margin (PM)



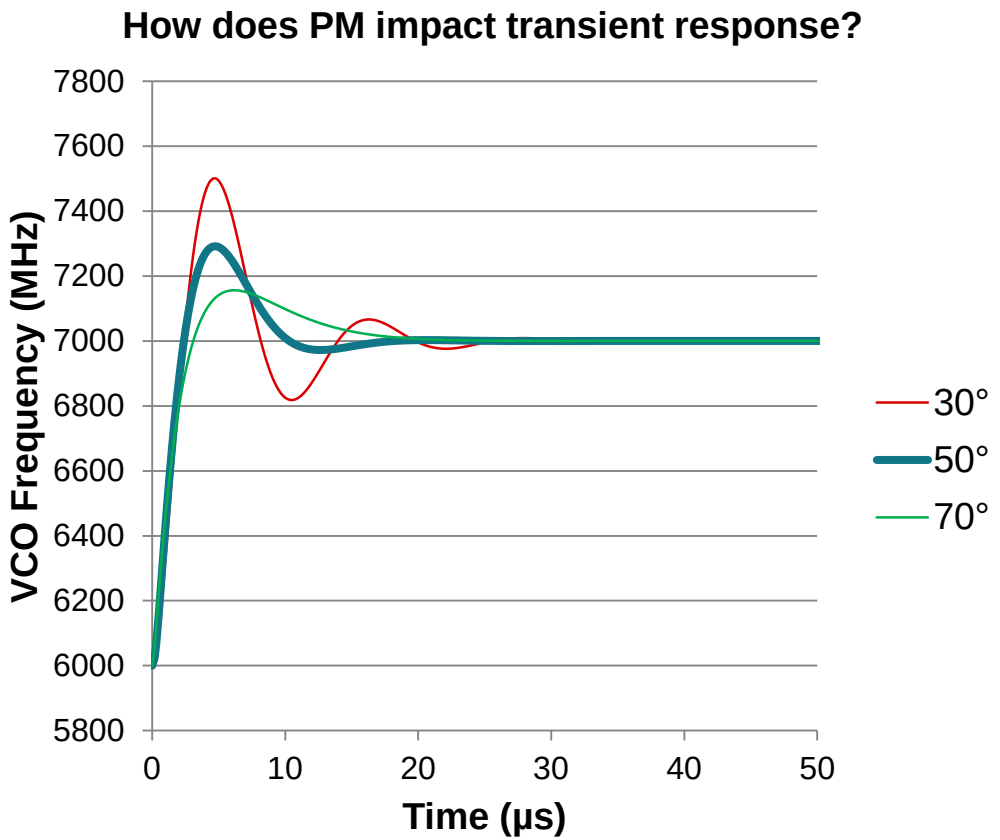
PM = 180 + phase at BW frequency offset

Phase margin’s impact on lock time



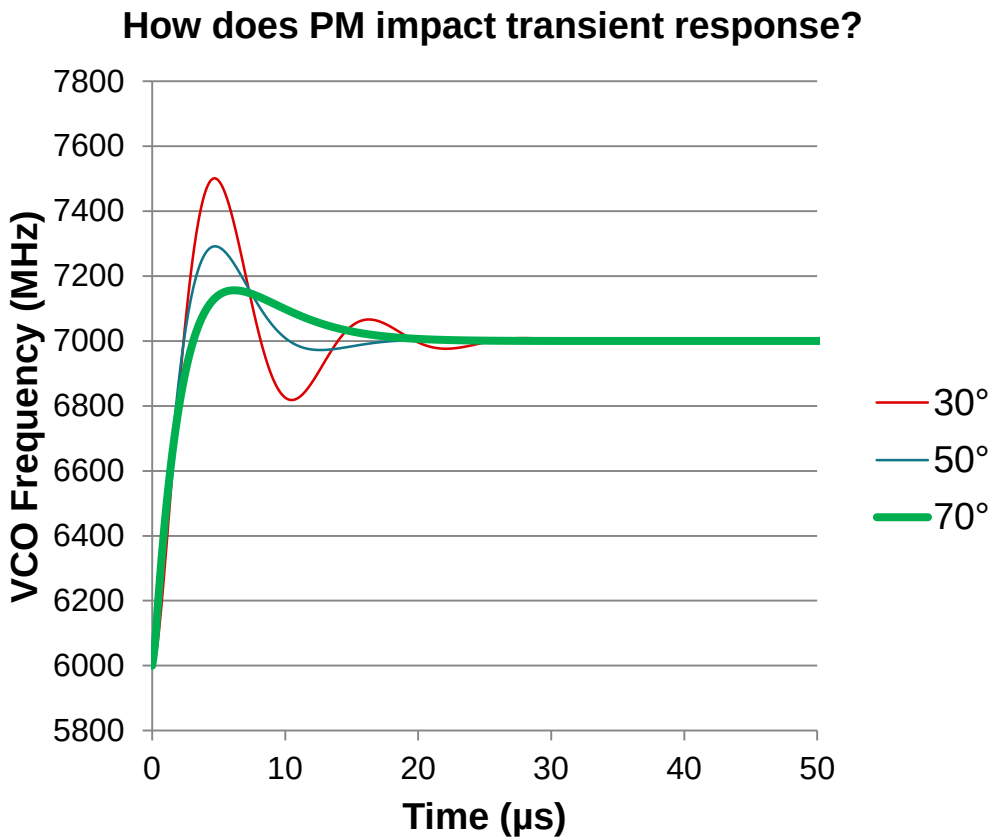
Phase margin	Why choose this?
30° - 45°	Reduce spurs

Phase margin's impact on lock time



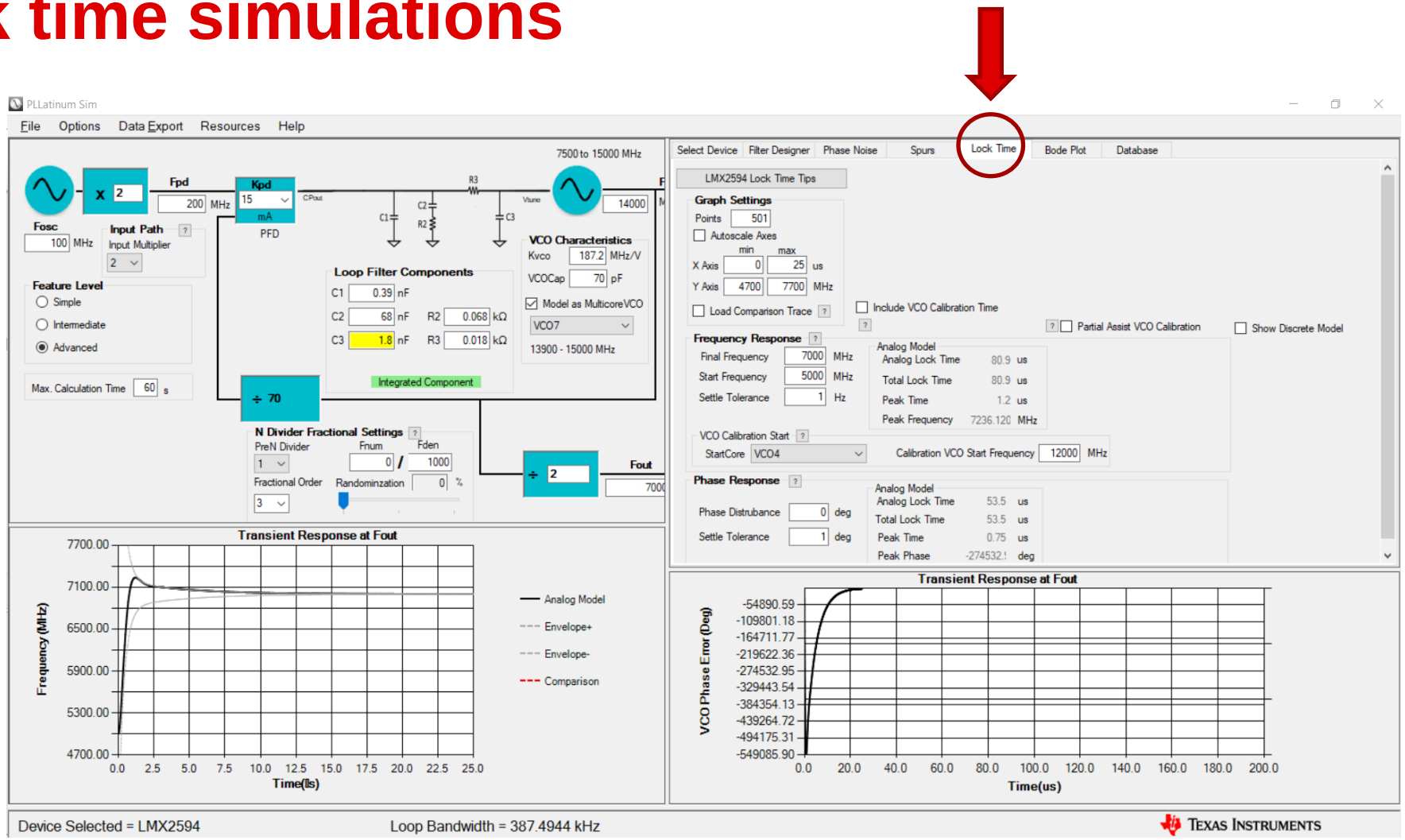
Phase margin	Why choose this?
30° - 45°	Reduce spurs
45° - 55°	Balanced lock time, phase noise and spurs

Phase margin's impact on lock time

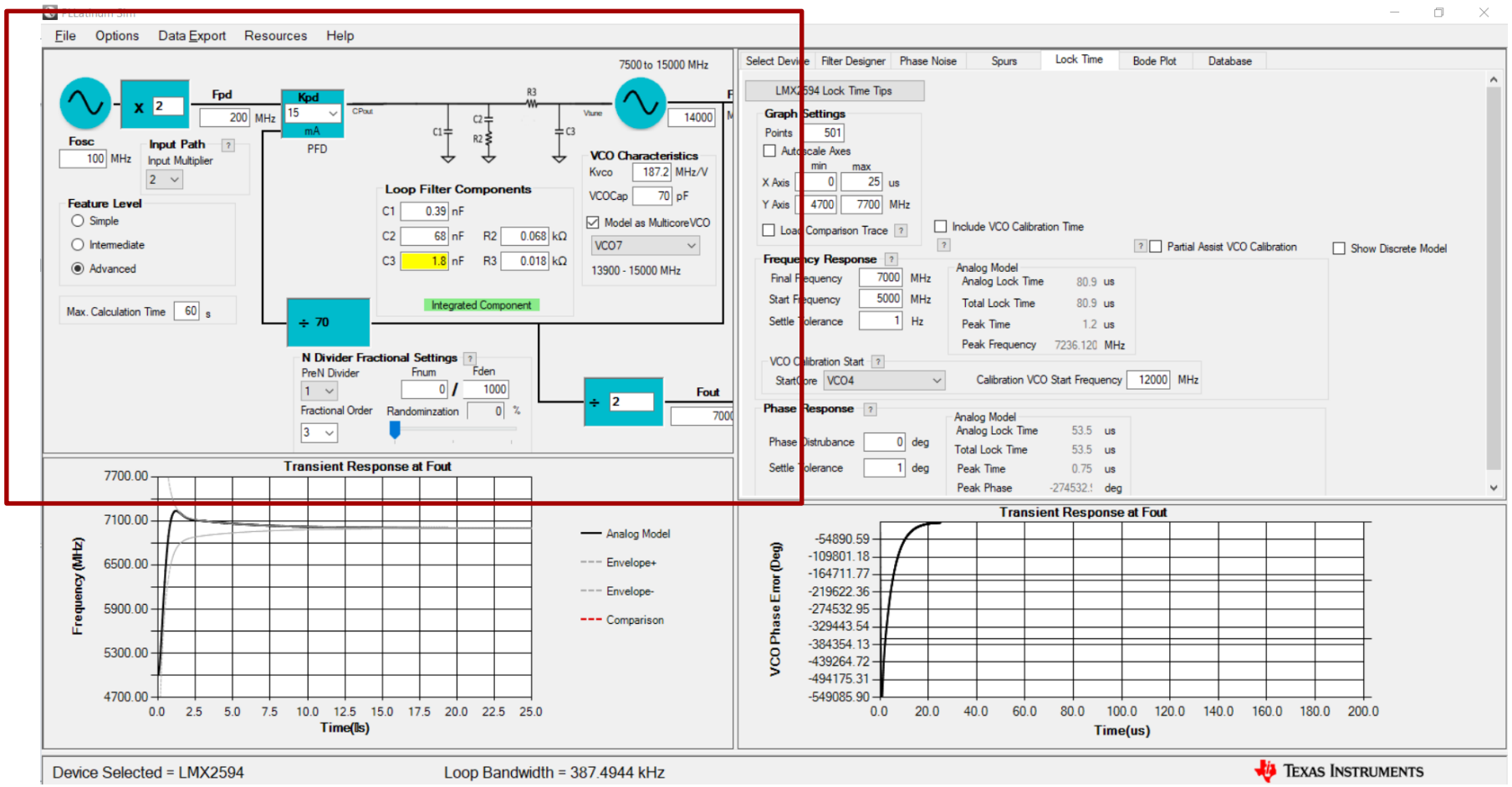


Phase margin	Why choose this?
30° - 45°	Reduce spurs
45° - 55°	Balanced lock time, phase noise and spurs
55° - 80°	Minimize jitter

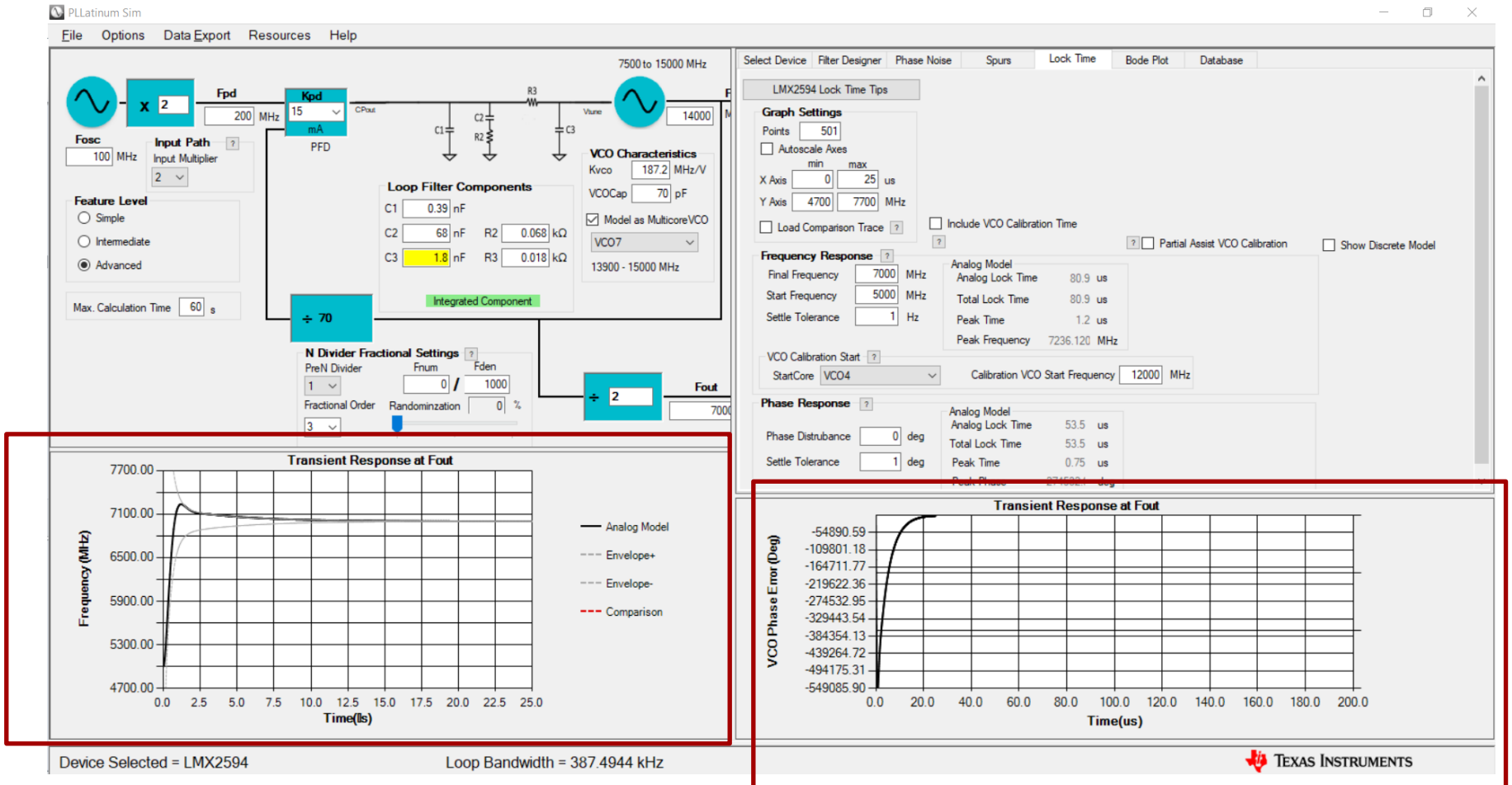
Lock time simulations



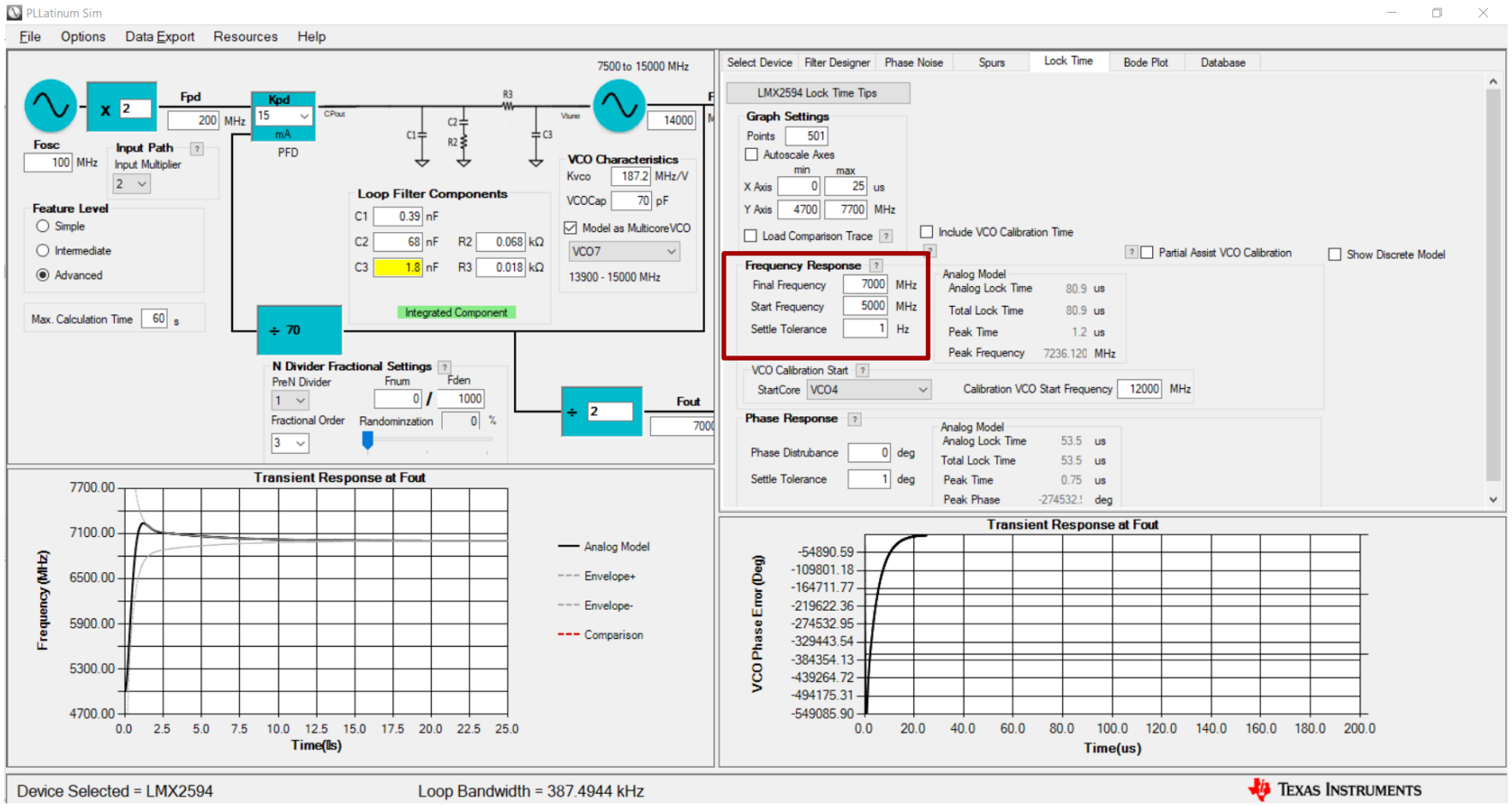
Lock time simulations



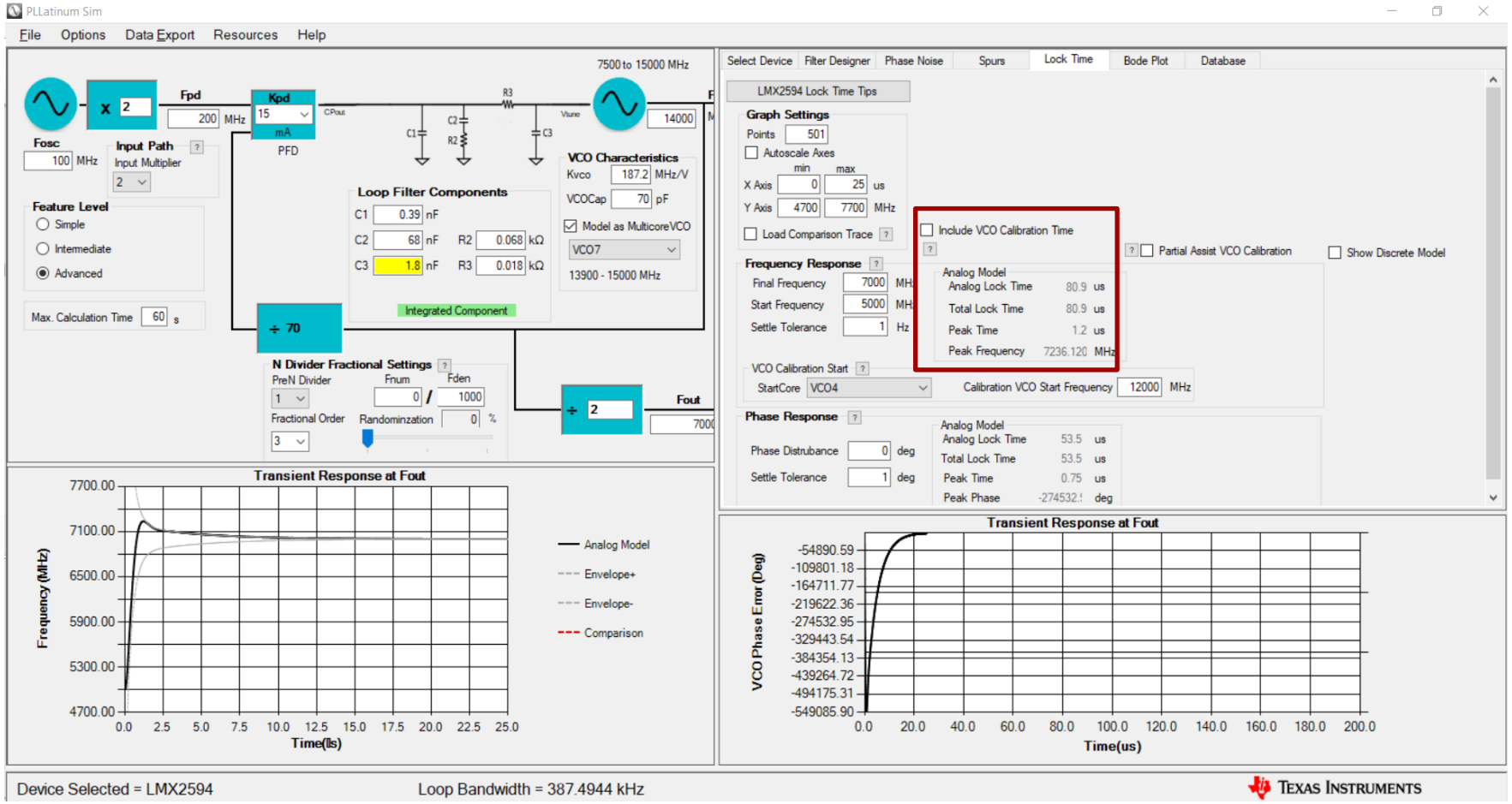
Lock time simulations



Lock time simulations



Lock time simulations



SNAA336: Streamline RF Synthesizer VCO Calibration and Optimize PLL Lock Time

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Quiz

- **True or false: The phase margin is the phase of the open loop transfer function when the gain of the PLL is equal to 0 dB.**

- **True or false: Phase margins under 30º should be avoided to enhance the stability of the PLL, and minimize ringing.**

- **True or false: Larger bandwidths lead to shorter lock times.**

Quiz

- **True or false: The phase margin is the distance of the phase from -180 degrees when the gain of the PLL is equal to 0 dB.**

- **True or false: Phase margins under 30º should be avoided to enhance the stability of the PLL, and minimize ringing.**

- **True or false: Larger bandwidths lead to shorter lock times, as the PLL can adjust to changes in the output frequency faster.**

Quiz

- True or false: When designing a loop filter for a tunable frequency range, the filter should be designed to meet a loop gain constant equal to the arithmetic mean of the minimum and maximum values the loop gain constant takes for the range of VCO frequencies selected.
- True or false: The zero of the transfer function, T2, is independent of the loop filter order and is always equal to R2 times C2 for a passive loop filter.
- True or false: When a device has integrated loop filter components, no external loop filter components need to be added to the schematic.

Please read the following sentences and determine if each statement is true or false. The next page will have the answers.

Quiz

- True or **false**: When designing a loop filter for a tunable frequency range, the filter should be designed to meet a loop gain constant equal to the arithmetic mean of the minimum and maximum values the loop gain constant takes for the range of VCO frequencies selected.
- **True** or false: The zero of the transfer function, T2, is independent of the loop filter order and is always equal to R2 times C2 for a passive loop filter.
- True or **false**: When a device has integrated loop filter components, no external loop filter components need to be added to the schematic.

Statement 1:

False – The loop filter should be designed for the ***geometric*** mean of the minimum and maximum values the loop gain constant takes, not the arithmetic mean.

Statement 2:

True – The zero of the transfer function, T2, is independent of the loop filter order and is always equal to R2 times C2 for a passive loop filter.

Statement 3:

False – While a fully integrated loop filter is possible, sometimes only part of the loop filter will be integrated in the device. The parts of the loop filter that aren't on-chip will still need to be routed to externally.