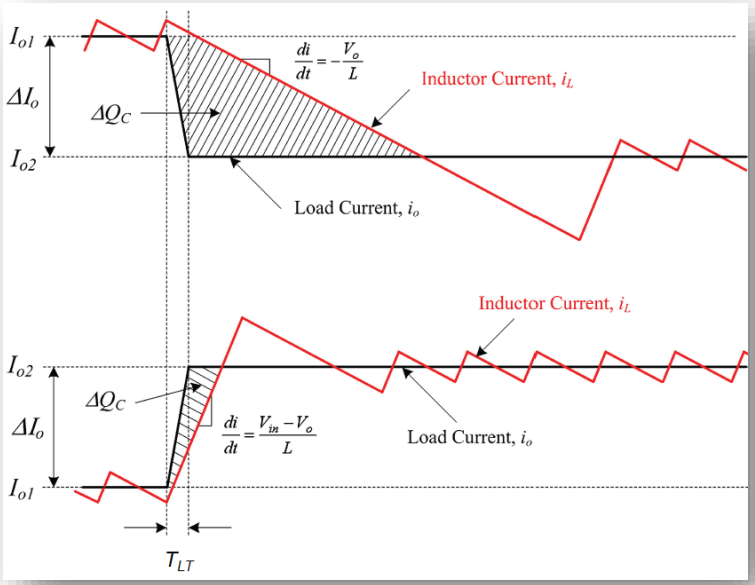
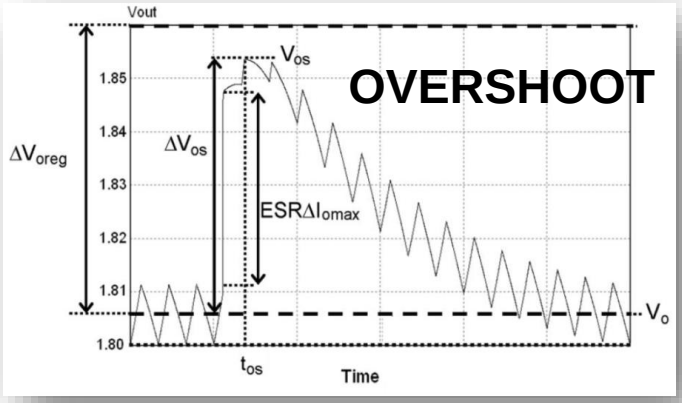
Switching Power Supply Component Selection

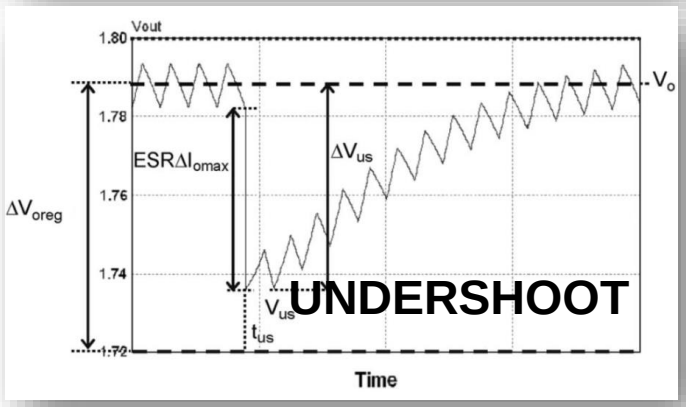
7.1e Capacitor Selection – Meeting Transient Response Requirements

Output Caps Selection: Load Transient

- The **overshoot** (or undershoot) occurs because of the **surplus** (or deficit) **of charge** in the output capacitor.
- Let's define the allowed variation for the output voltage as ΔV_{oreg}
- Because of slope constraints due to the inductor: **when D < 0.5 the overshoot is greater than the undershoot and vice versa when D > 0.5**

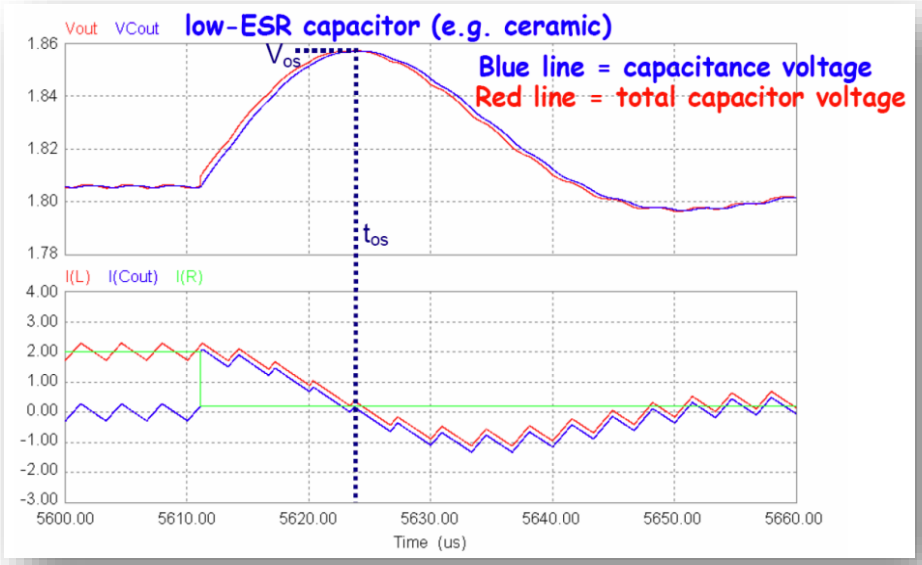


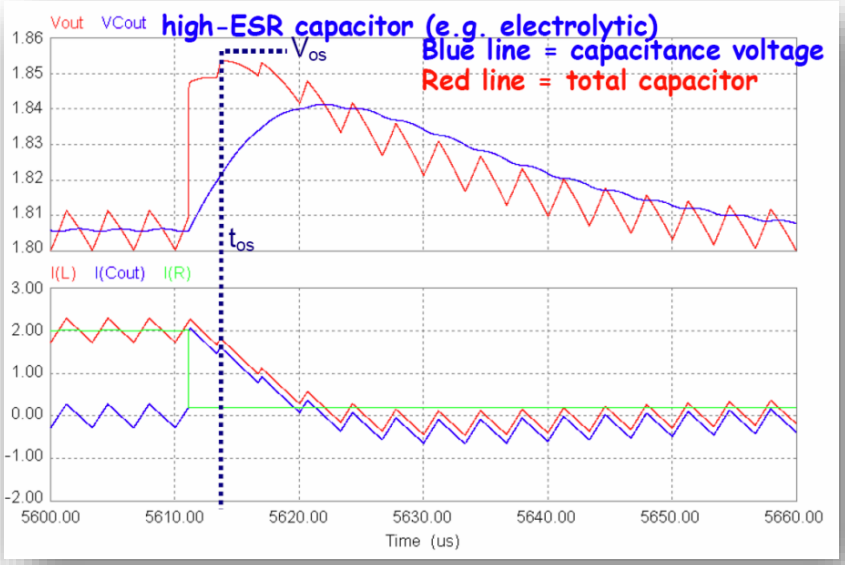




Load Transient Analysis

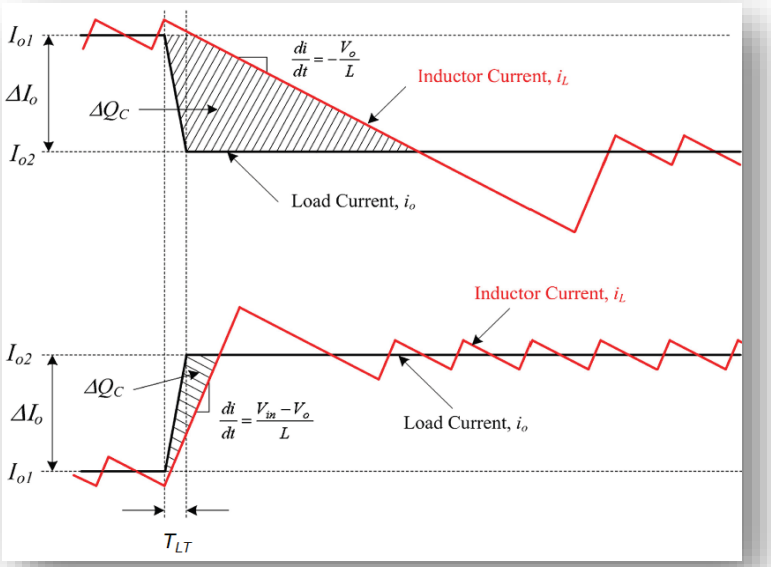
- The instant when the peak of the overshoot occurs depends on the type of the output capacitor.
- The exact point where peak overshoot is reached, and its magnitude, must be calculated by taking into account joined influence of C and ESR.





Load Transient Analysis

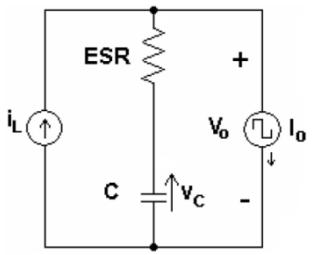
- Three different cases can be considered when load transient occurs:
  1. **Stepwise load transient**: load transient duration T_{LT} is much smaller than closed loop system's response time given by the crossover frequency f_C, $T_{LT} << 1/(4f_C)$
  2. **Fast load transient**: load transient duration T_{LT} is smaller than closed loop system's response time $T_{LT} < 1/(4f_C)$
  3. **Slow load transient**: load transient duration T_{LT} is larger that closed loop system's response time $T_{LT} > 1/(4f_C)$
- In 1st and 2nd case the control network is not able to compensate output voltage variations suddenly after a load variation. Hence, the output filter must be designed to keep the output voltage within the maximum allowed range in early time after the load transient until the loop has the chance to respond.



The impact of load transient constraint on the output capacitor size is lower in 3rd case. For this reason **worst case stepwise load transient is treated**. The output current slew rate will be considered as infinite (***T_{LT} = 0***). This is a reasonable assumption in application such FPGA supplies where load-current slew rate may range up to 100A/µs.

Load Transient Analysis

- Is it possible to analyze a buck converter during load transient by means of the following circuit
- t_{LT} is the instant when the load transient occurs, it can occur during ON time or during OFF time



$$r=\Delta i_{Lpp}/\Delta I_{omax}$$

$0<t_{LT}<DT_s$ **ON TIME**

$$i_C(t)=-\frac{\Delta i_{Lpp}}{2}+\Delta I_{o\max}+\frac{\Delta i_{Lpp} f_s}{D'}\left(\frac{t_{LT}}{D}-t\right)$$

$$v_o(t)=V_o-\frac{\Delta i_{Lpp}}{12C}\left(\frac{(1-2D)}{f_s}+6t_{LT}\left(1-\frac{f_s t_{LT}}{D}\right)\right)+ESR\,i_C(t)+\frac{1}{C}\int_{t_{LT}}^{t} i_C(\tau)d\tau$$

$$t_{os}=\frac{D'}{f_s}\left(\frac{1}{r}-\frac{1}{2}\right)-ESR\,C+\frac{t_{LT}}{D}$$

$$V_{os}=V_o+\frac{\Delta I_{o\max}}{2f_sCD'r}\left[D^2\left(1-\frac{1}{12}r^2\right)-r\left(1-\frac{1}{12}r\right)+(1-2D)+rD(2-D)+\right.$$
$$\left.+(ESRf_sCr)^2+rf_s\left(r+2(D-2)+\frac{1}{D}(2-r)\right)t_{LT}+r^2f_s{}^2\frac{D'}{D^2}t_{LT}{}^2\right]$$

$DT_s<t_{LT}<T_s$ **OFF TIME**

$$i_C(t)=\frac{\Delta i_{Lpp}}{2}+\Delta I_{o\max}+\frac{\Delta i_{Lpp}}{D'}\cdot(D-f_st)$$

$$v_o(t)=V_o-\frac{\Delta i_{Lpp}}{2C}\left(\frac{1}{6D'f_s}(3D+2D^2+1)-\left(1+\frac{2D}{D'}\right)t_{LT}-\frac{t_{LT}{}^2f_s}{D'}\right)+ESRi_C(t)+\frac{1}{C}\int_{t_{LT}}^{t} i_C(\tau)d\tau$$

$$t_{os}=\frac{1}{f_s}\left(\frac{(1+D)}{2}+\frac{D'}{r}\right)-ESR\,C$$

$$V_{os}=V_o+\frac{\Delta I_{o\max}}{2f_sCD'r}\left[r(1-D^2)\left(1+\frac{1}{12}r\right)-D^2+(ESRf_sCr)^2-2rf_sD't_{LT}\right]$$

- **Worst case condition** occurs when:
  - $t_{LT} = DT_S$ for ***overshoot***
  - $t_{LT} = T_S$ for ***undershoot***

Let's assume a high cross over frequency controller. Minimum duty cycle is assumed to be 0 and maximum duty cycle is assumed to be 1.

Load Transient Analysis: Overshoot

- Assuming that the step down load transient occurs at $\mathbf{t_{LT} = DT}$ (overshoot worst case), the instant of peak variation of the output voltage and its maximum overshoot peak value are given by:

$$t_{os} = T_s\left(\frac{1}{2}(1+D)+\frac{D'}{r}\right) - ESR\,C$$

$$v_o(t_{os}) = V_o + \frac{\Delta I_{o\max}}{f_s C D' r}\cdot\left(D'^2(1+r)+\frac{1}{12}r^2(1-D^2)+(ESR\,r\,f_s C)^2\right)$$

- If $\mathbf{t_{os} = DT_s}$ the magnitude of V_{OS} is determined by ESR only (high ESR case $\boldsymbol{ESR_H}$)
- If $\mathbf{t_{os} > DT_s}$ the magnitude of V_{OS} jointly depends on C and ESR values (low ESR case $\boldsymbol{ESR_L}$)

$$\Delta V_{oreg} - (v_o(DT_s) - V_o) = ESR\,\Delta I_{o\max} \qquad \underline{t_{os}=DTs}$$

$$\Delta V_{oreg} = V_{os} - V_o \qquad \underline{t_{os}>DTs}$$

$$T_s\left(\frac{1}{2}(1+D)+\frac{D'}{r}\right) - ESR\,C = D\,T_s$$

$$ESR_H = \frac{1}{2+r}\left(2R_{LT} + \frac{r(1-2D)}{6 f_s C}\right)$$

$$ESR_L = \frac{\sqrt{D'\left(2rR_{LT}f_sC - (1+r)D' - \frac{1}{12}r^2(1+D)\right)}}{r f_s C}$$

$$ESR_{crit} = \frac{D'}{f_s C}\left(\frac{1}{r}+\frac{1}{2}\right)$$

$R_{LT} = \Delta V_{oreg}/\Delta I_{omax}$

Load Transient Analysis: Overshoot

$$ESR_H = \frac{1}{2+r}\left(2R_{LT} + \frac{r(1-2D)}{6 f_s C}\right)$$

$$ESR_L = \frac{\sqrt{D'\left(2rR_{LT} f_s C - (1+r)D' - \frac{1}{12}r^2(1+D)\right)}}{r f_s C}$$

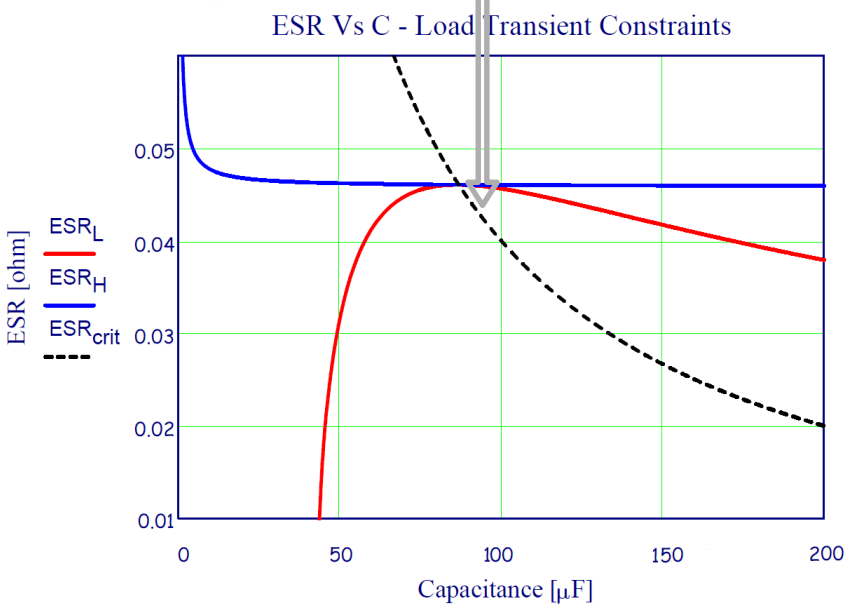
$$ESR_{crit} = \frac{D'}{f_s C}\left(\frac{1}{r} + \frac{1}{2}\right)$$

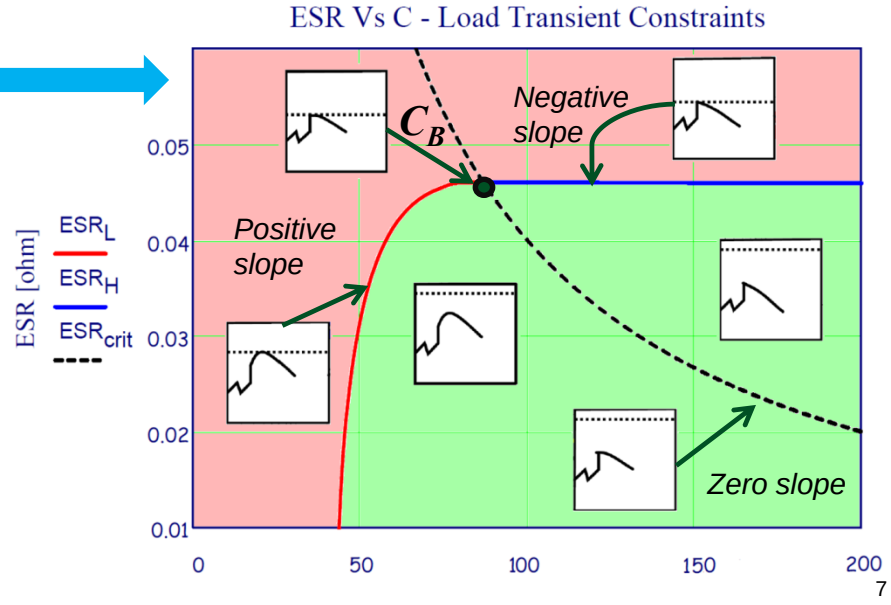
$R_{LT} = \Delta V_{oreg} / \Delta I_{omax}$

- The three curves cross at the boundary value of capacitance C_B given by:

$$C_B = \frac{1}{f_s R_{LT} r}\left(\frac{r^2}{12}(1+D') + D'(1+r)\right)$$

- A real capacitor whose values of ESR and C correspond to a point located below this curve (**green area**) can be considered suitable to maintain the output voltage within the given regulation window in presence of a charging load transient.





Load Transient Analysis: Overshoot

- It makes sense to consider the effect of stray inductances $L_{ESL} = ESL + L_{PCB}$ only it the real slew-rate SR of the load current transition is known.

$$\Delta V_o(t_r) = \Delta I_{o\max} ESR + L_{\mathrm{esl}} SR$$

$$t_r = t_{\mathrm{LT}} + \Delta I_{o\max} / SR$$

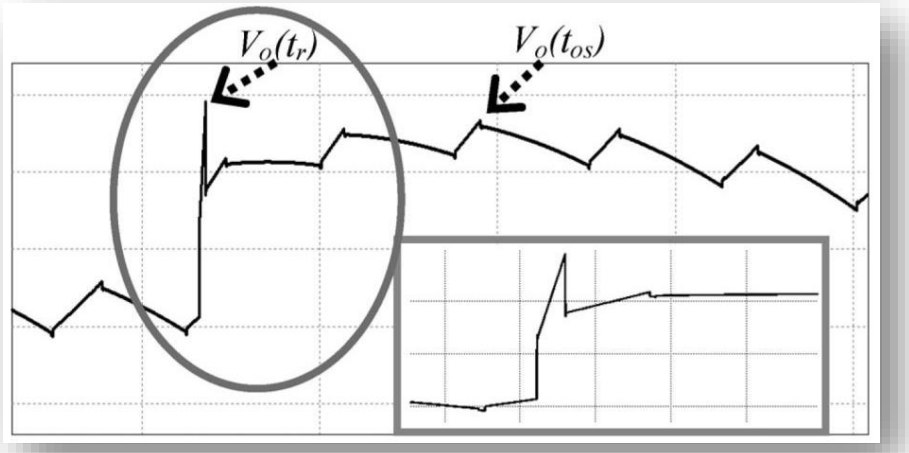
- After the instant t_r, the output voltage evolves in the time as if there was no ESL.

- Load transient constraints are met if C, ESR and ESL are such that both conditions are fulfilled:

$$\Delta V_O(t_r) < \Delta V_{Oreg}$$
$$\Delta V_O(t_{os}) < \Delta V_{Oreg}$$

- The effect of L_{ESL} can be accounted by including the following constraints for the ESR

$$ESR_{\max} = \frac{\Delta V_{Oreg} - L_{\mathrm{esl}} SR}{\Delta I_{o\max}}$$



Overshoot

- L_{ESL} = 10nH
- SR = 3 A/µs

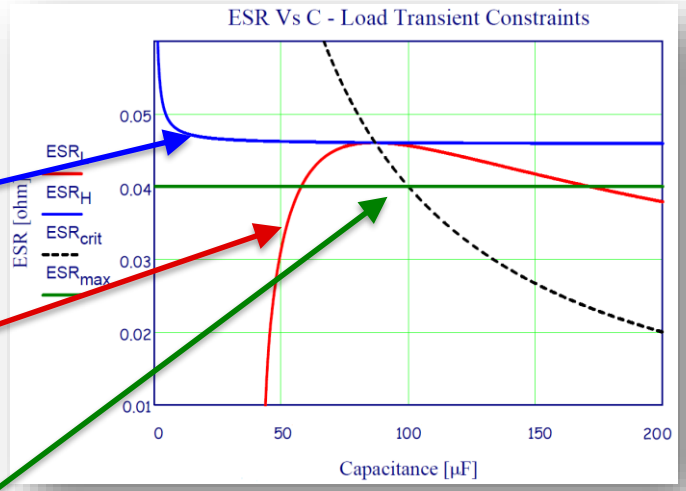
$$ESR_H = \frac{1}{2+r}\left(2R_{LT} + \frac{r(1-2D)}{6 f_s C}\right)$$

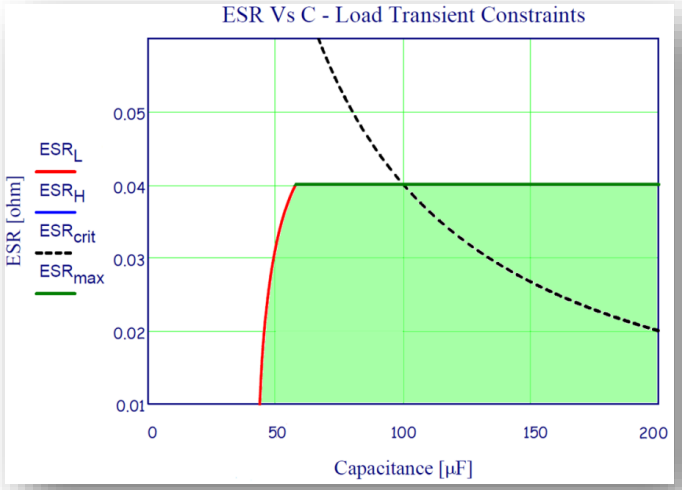
$$ESR_L = \frac{\sqrt{D'\left(2rR_{LT} f_s C - (1+r)D' - \frac{1}{12} r^2 (1+D)\right)}}{r f_s C}$$

$$ESR_{crit} = \frac{D'}{f_s C}\left(\frac{1}{r} + \frac{1}{2}\right)$$

$R_{LT} = \Delta V_{oreg} / \Delta I_{omax}$

$$ESR_{max} = \frac{\Delta V_{Oreg} - L_{esl} SR}{\Delta I_{o\,max}}$$





Load Transient Analysis Overshoot: Simplified Equation

- It is possible to derive **simplified boundaries** for C and ESR.
- Let's assume that the minimum output capacitance required is C_B previously defined as:

$$C_{min} = C_B = \frac{\Delta I_{omax}^{\,2}}{f_s \times \Delta V_{oreg} \times \Delta i_{Lpp}} \times \left[\left(\frac{\Delta i_{Lpp}}{\Delta I_{omax}} \right)^2 \times \frac{1 + D'}{12} + D' \times \left(1 + \frac{\Delta i_{Lpp}}{\Delta I_{omax}} \right) \right]$$

- It is possible to calculate the maximum allowed value of the ESR by replacing $\boldsymbol{C_B}$ value into the $\boldsymbol{ESR_{crit}}$ formula previously defined:

$$ESR_{max} = \frac{D'}{f_s \times C_B} \times \left(\frac{\Delta I_{omax}}{\Delta i_{Lpp}} + \frac{1}{2} \right)$$

- Any capacitor whose value of capacitance and ESR is higher than $\boldsymbol{C_{min}}$ and lower the $\boldsymbol{ESR_{max}}$ is suitable to meet load transient requirements for a buck converter.

Thank you!