UART Protocol Overview

TI Precision Labs – Microcontrollers

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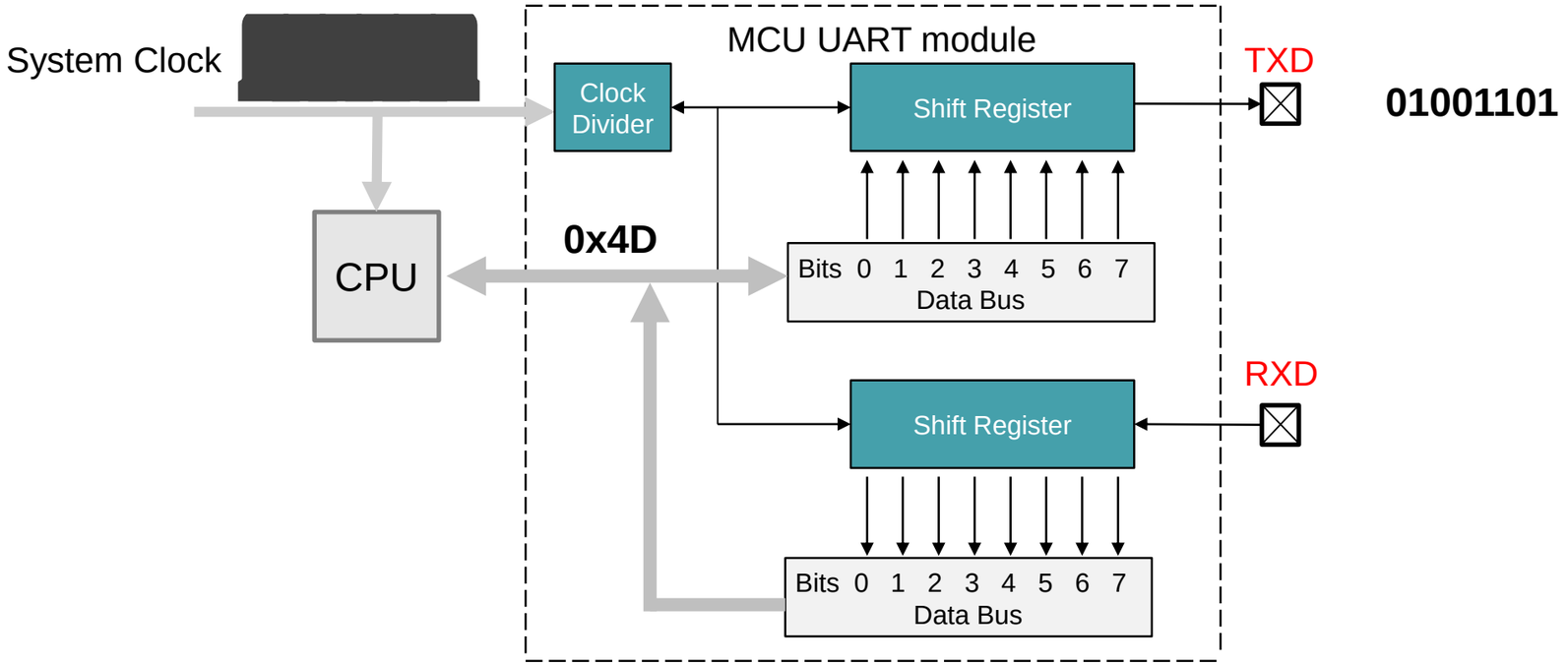
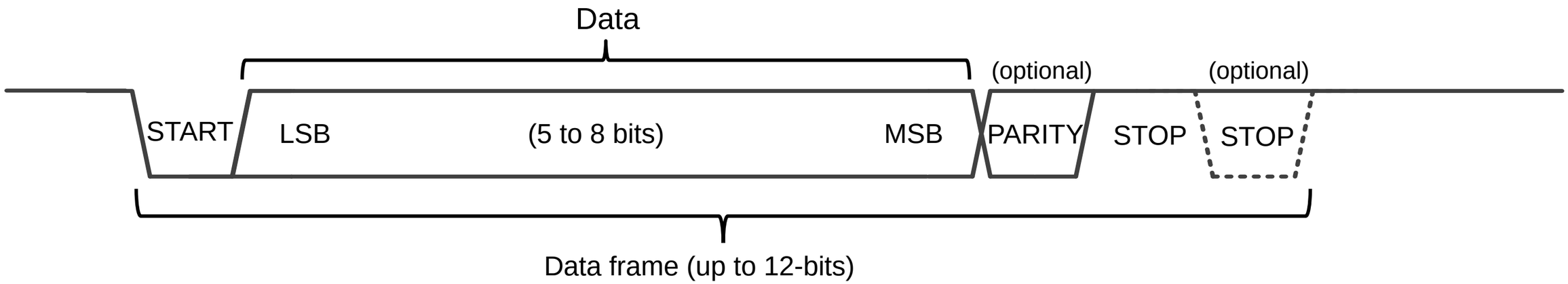
The UART

- UART – Universal Asynchronous Receiver Transmitter
- Requires only 2-pins, RXD and TXD
- No additional synchronization pin or clock signal is needed
- Synchronization by adding START and STOP bits to data



UART Hardware Protocol

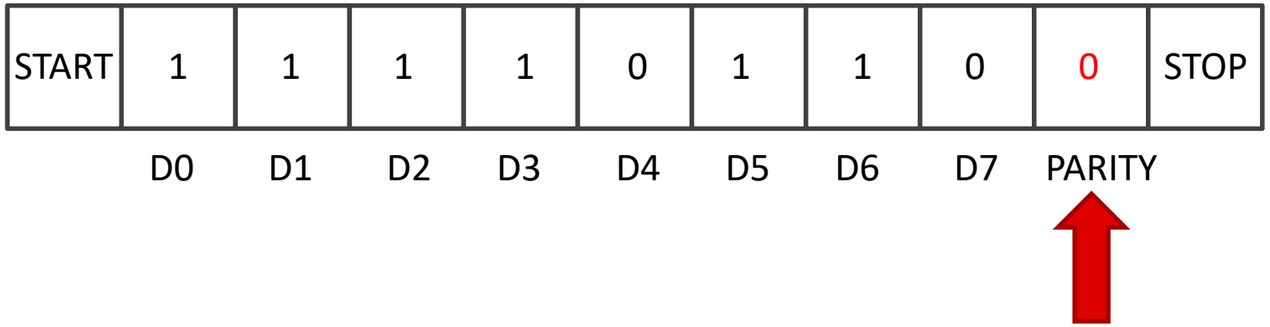
- UART Data Frame
- Start bit – synchronizes receiver to start of frame
- Data bits - data
- Parity bit – single bit error detection (optional)
- Stop bit –signals end of the frame
- Second Stop bit (optional)



UART Parity Example

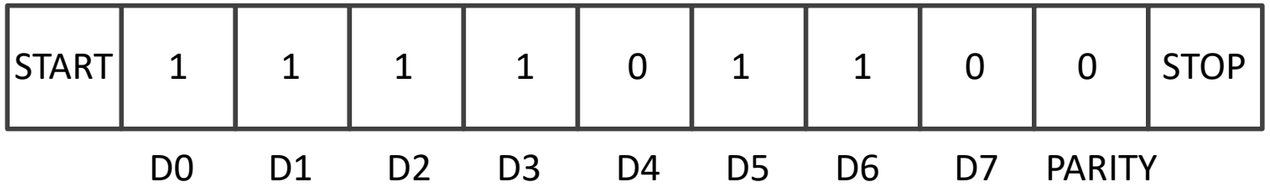
- PARITY provides single bit error detection (optional)
- PARITY options are Even, Odd, None
- Both UARTs must be configured the same
- Transmitter generates PARITY bit
  - Even Parity configuration
  - Sum of frame = 6 (even)
  - PARITY bit set to 0

1+1+1+1+0+1+1+0 = 6 so PARITY bit set to 0



- Received packet
  - Count number of ‘1’s
  - Add PARITY bit value
  - If sum is even, data is valid

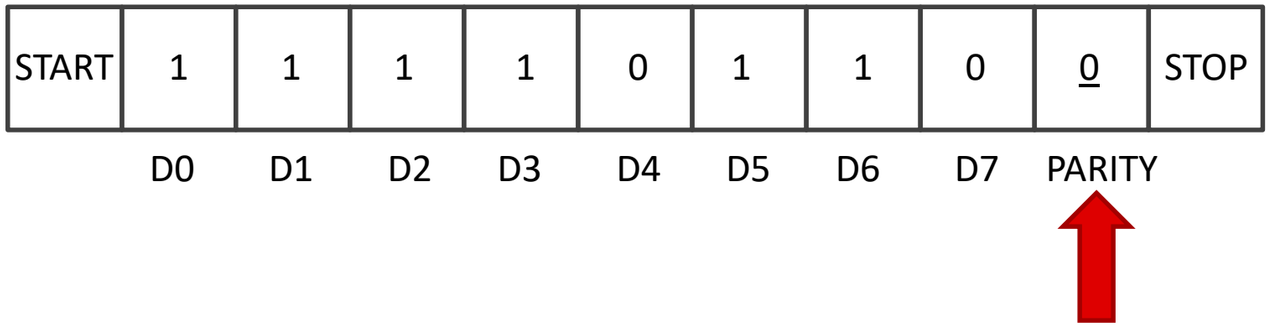
1+1+1+1+0+1+1+0 = 6 + 0 (parity) = 6, so data is valid



UART Parity Example – Error Detected

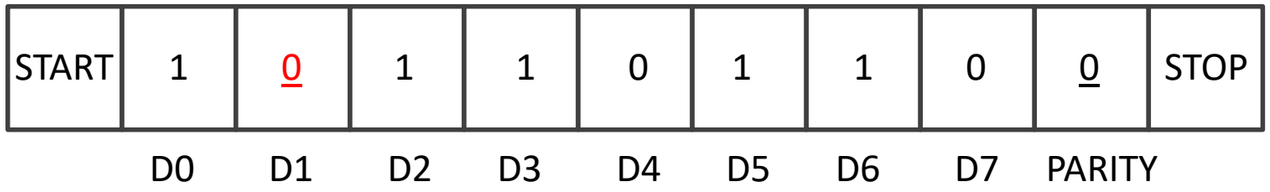
- Transmitter generates PARITY bit
  - Even parity configuration
  - Sum of frame = 6
  - PARITY bit set to 0

1+1+1+1+0+1+1+0 = 6, PARITY bit set = 0



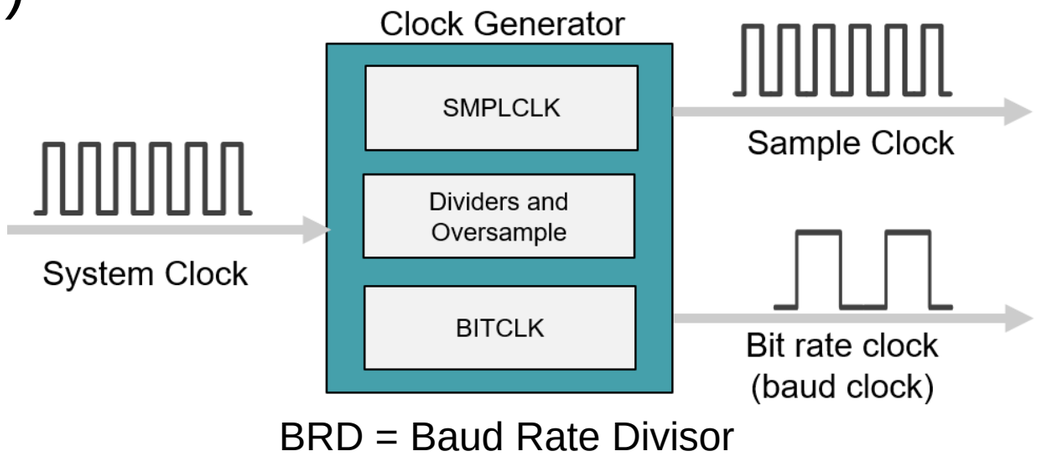
- Received packet
  - Noise changes bit D1
  - Count number of ‘1’s
  - Add PARITY bit value
  - Sum is odd, data is not valid
  - Parity error flag set

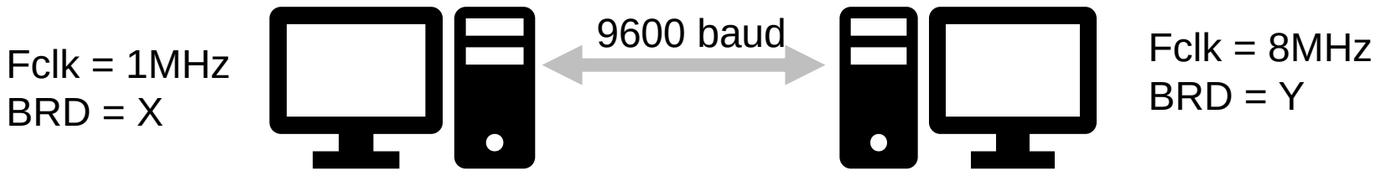
1+0+1+1+0+1+1+0 = 5 + (PARITY bit) = 5, so bit error



Baud Rates

- Common Baud Rates are 9600, 19200, 115200
- UARTs must use same baud rate
- System clock and Baud Rate Divisor (BRD)



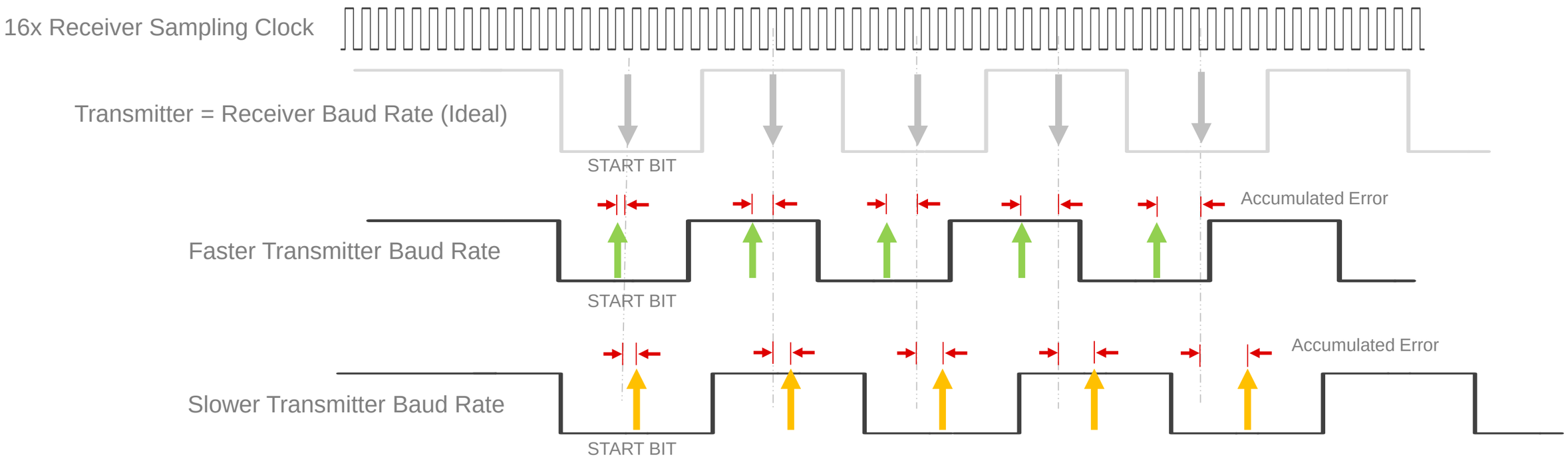


Baud Rate - Maximum Error Tolerance

- Typical maximum baud rate error tolerance is 2-3%
- Bit error accumulation
- START bit synchronization
- RX Signal rise and fall times

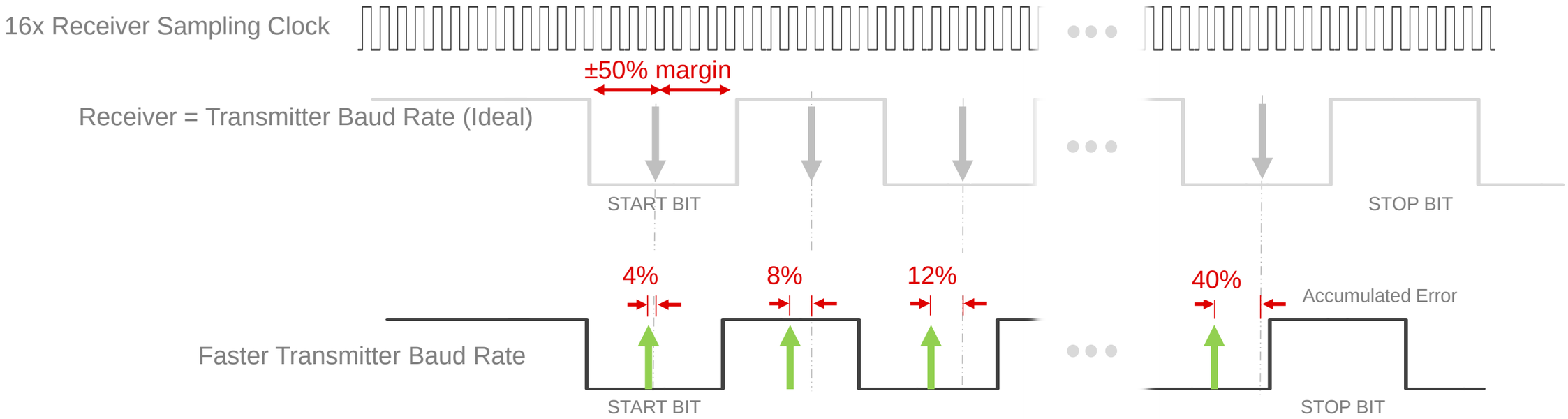
Baud Rate Accumulation Errors

- Receiver uses oversample clock (16x baud rate clock)
- Faster baud
- Slower baud rate



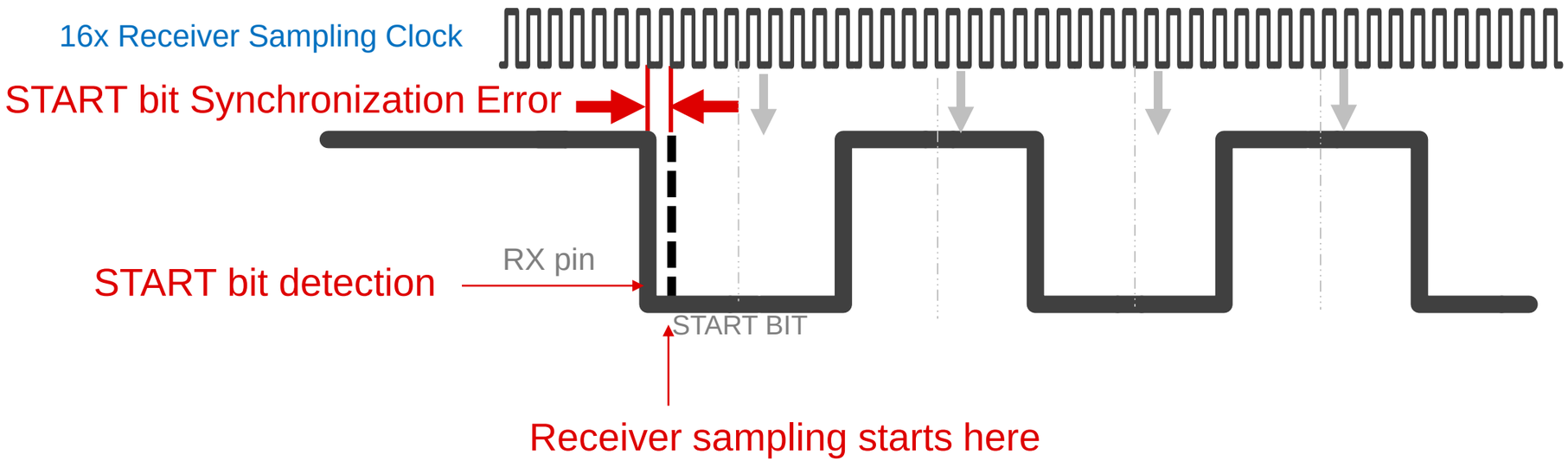
Baud Rate Accumulation Errors

- Theoretical Maximum Accumulated bit tolerance
- Bit error margin or margin of error
- Example with a faster clock:
  - Accumulated error = ± 40% over 10 bit periods



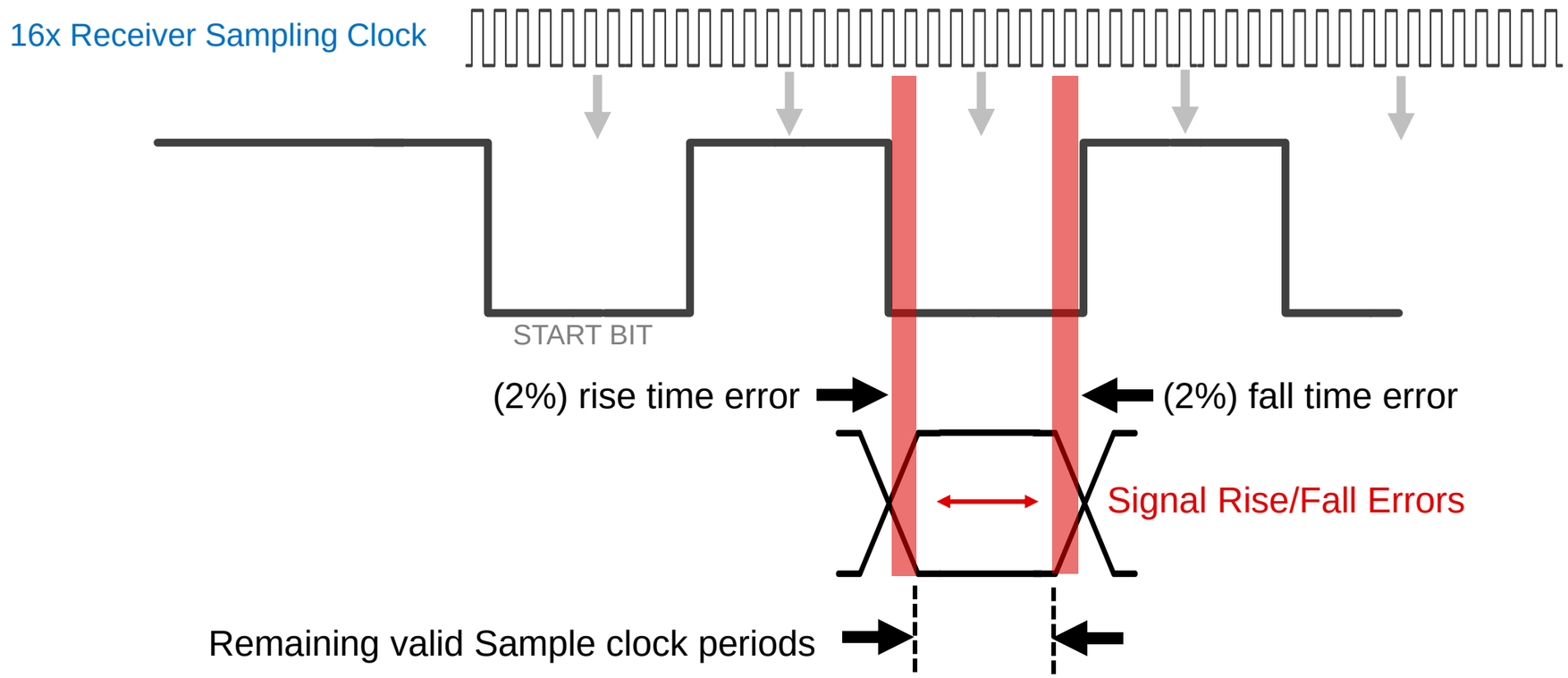
Start bit Synchronization Error

- START bit falling edge
- Sampling clock synchronization tolerance
- 1/16 clock cycle or 6.25% of the START bit period

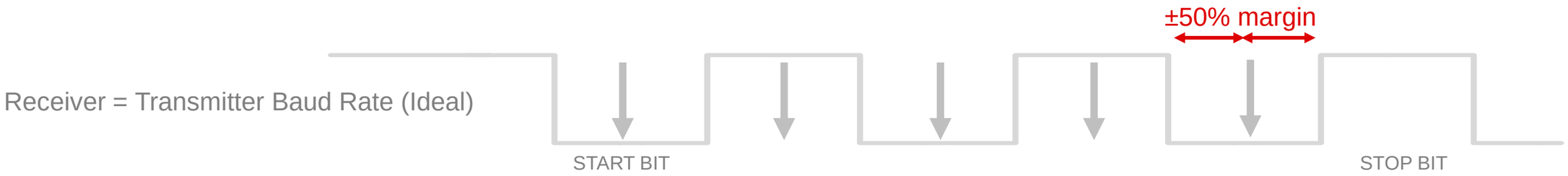


RX Signal slew rate (rise/fall times)

- Rise/Fall timing delays
- Caused by added capacitance



Example Baud Rate Error Tolerance Calculation



Example calculation

Find actual margin:

50%	-	6.25%	-	2%	=	41.75%
Ideal Margin		Synchronization error		Rise/fall error		Actual margin

Calculate baud rate margin:

41.75%	÷	10	=	±4.175%
Margin		Number of bits/frame		Baud rate margin

Transmitter and receiver clock can vary by 4.175% without any bit errors

Summary

- UART Interface and Synchronization
- UART Hardware Protocol
- Parity Examples
- Baud rate calculations

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