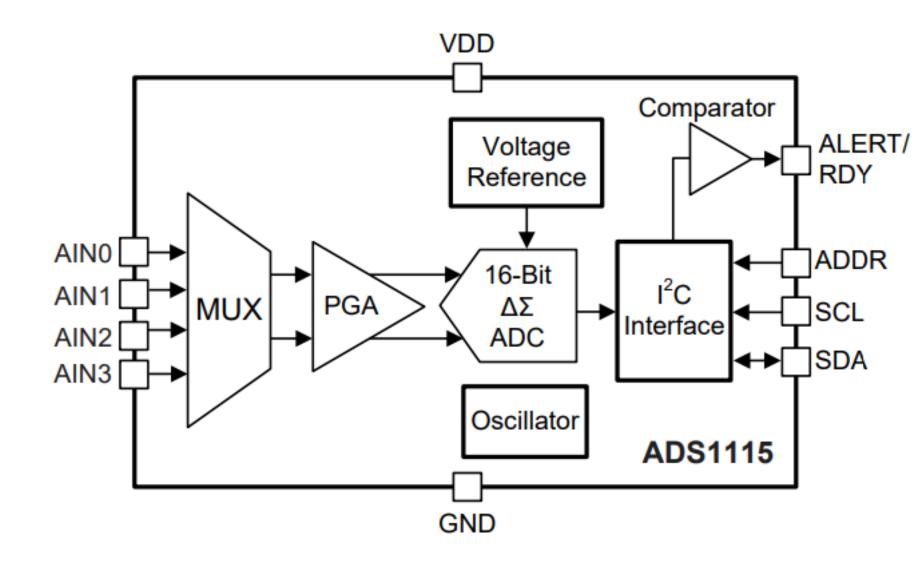
Basics of I2C: An I2C Example TIPL 6102 TI Precision Labs – Digital Communication

Prepared by Joseph Wu Presented by Alex Smith

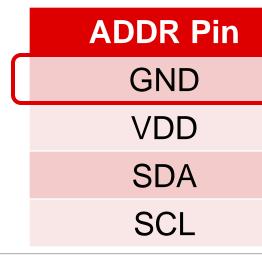






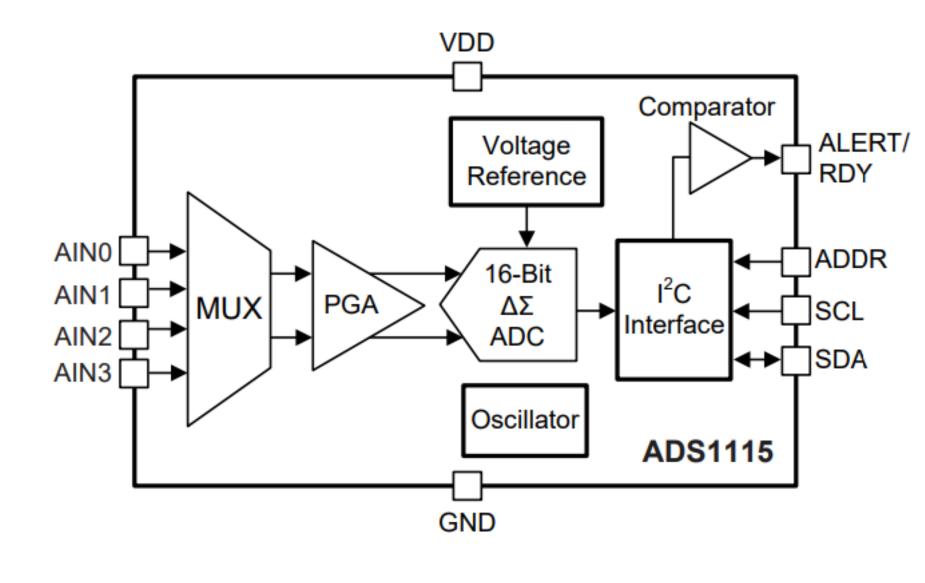
I2C Example

I2C address is pin configurable Device has four internal registers



Precision ADC with PGA, adjustable data rates, and multiplexer input

I2C Address 100 1000 (48h) 100 1001 (49h) 100 1010 (4Ah) 100 1011 (4Bh) **TEXAS INSTRUMENTS** 2



I2C Example

I2C address is pin configurable

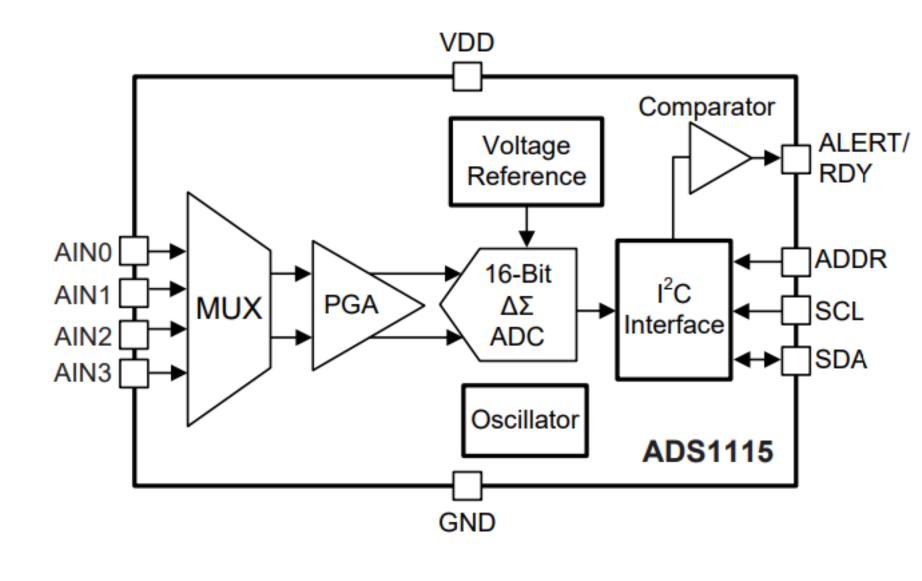
Pointer	
00	Con
01	Con
10	Lo_
11	Hi_t

Precision ADC with PGA, adjustable data rates, and multiplexer input

Device has four internal registers

Register

- version data
- nfiguration
- threshold register
- threshold register



I2C Example

I2C address is pin configurable

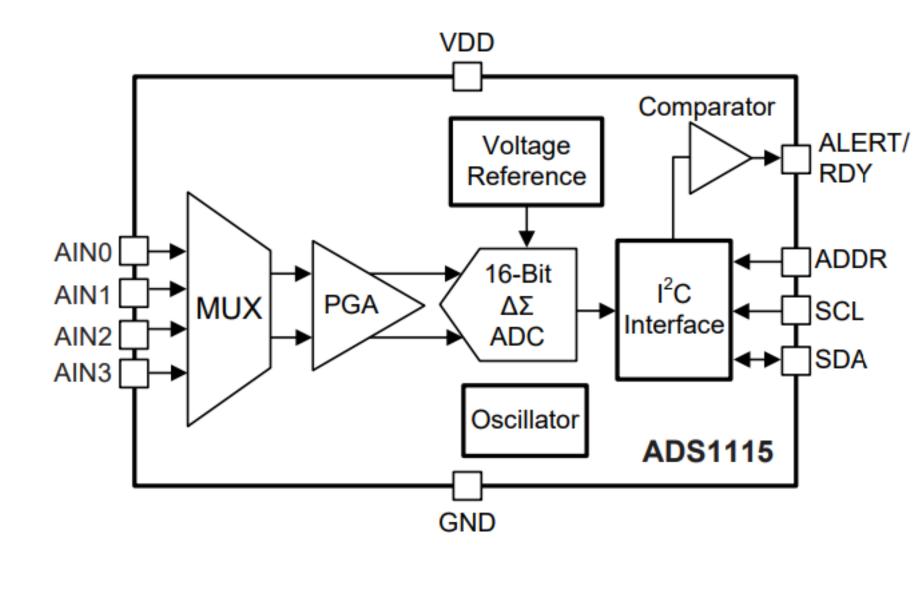
	Pointer	
	00	Con
$\left[\right]$	01	Con
	10	Lo_
	11	Hi_t

Precision ADC with PGA, adjustable data rates, and multiplexer input

Device has four internal registers

Register

- nversion data
- nfiguration
- threshold register
- threshold register



I2C Example

I2C address is pin configurable

Pointer	
00	Con
01	Con
10	Lo_
11	Hi_t

Precision ADC with PGA, adjustable data rates, and multiplexer input

Device has four internal registers

Register

- nversion data
- nfiguration
- threshold register
- threshold register

Figure 36. Config Register

-							
	15	14	13	12	11	10	9
[OS		MUX[2:0]			PGA[2:0]	
[R/W-1h		R/W-0h			R/W-2h	
	7	6	5	4	3	2	1
		DR[2:0]		COMP_MODE	COMP_POL	COMP_LAT	COMP_C
I		R/W-4h		R/W-0h	R/W-0h	R/W-0h	R/W



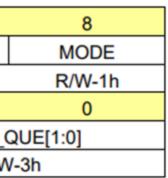
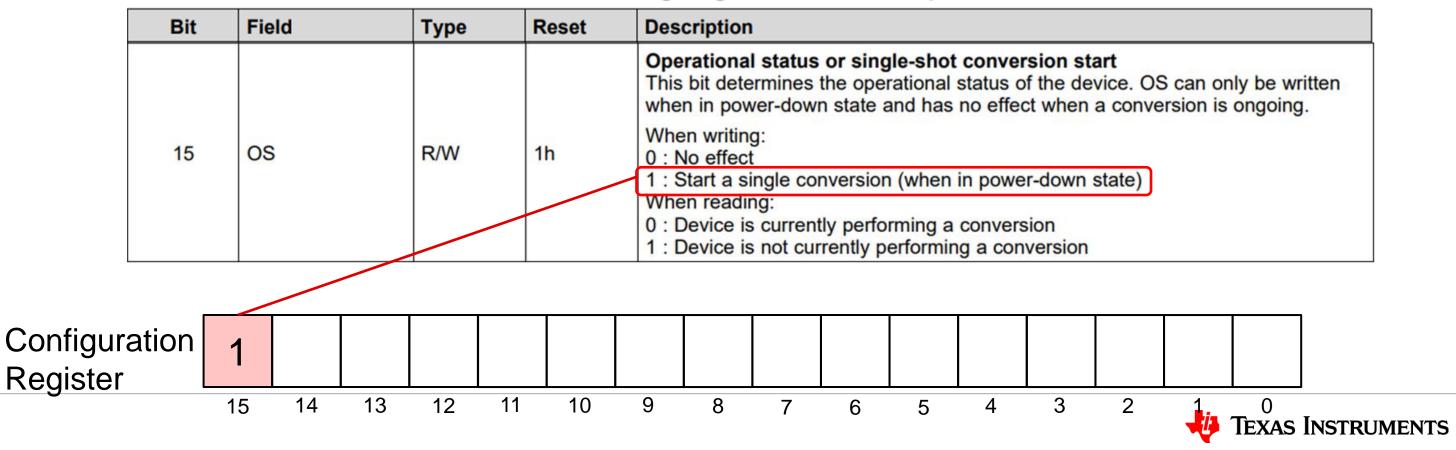




Figure 36. Config Register

	15	14	13	12	11	10	9
	OS		MUX[2:0]			PGA[2:0]	
	R/W-1h		R/W-0h			R/W-2h	
	7	6	5	4	3	2	1
		DR[2:0]		COMP_MODE	COMP_POL	COMP_LAT	COMP_C
I		R/W-4h		R/W-0h	R/W-0h	R/W-0h	R/W

Table 8. Config Register Field Descriptions





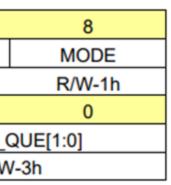
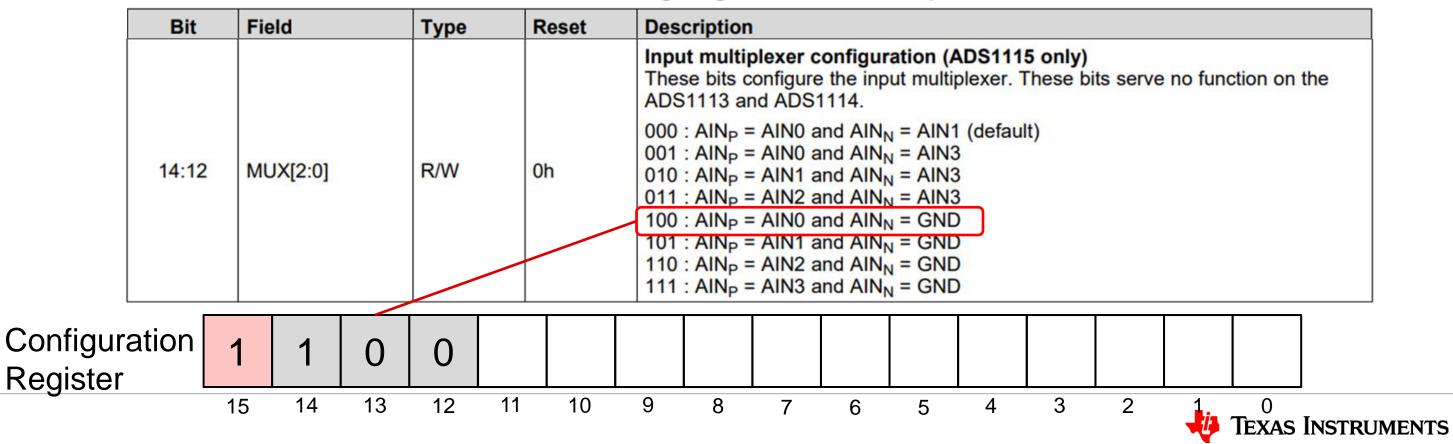


Figure 36. Config Register

15 14 13 12 11 10 9 OS MUX[2:0] PGA[2:0] PGA[2:0] <th></th>	
R/W-1h R/W-0h R/W-2h	
7 6 5 4 3 2 1	
DR[2:0] COMP_MODE COMP_POL COMP_LAT COMP	<u>ە_</u> ر
R/W-4h R/W-0h R/W-0h R	R/W





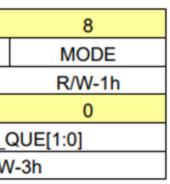
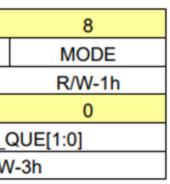


Figure 36. Config Register

15 14 13 12 11 10 9 OS MUX[2:0] PGA[2:0] PGA[2:0] <th></th>	
R/W-1h R/W-0h R/W-2h	
7 6 5 4 3 2 1	
DR[2:0] COMP_MODE COMP_POL COMP_LAT COMP	<u>ە_</u> ر
R/W-4h R/W-0h R/W-0h R	R/W

	Bit	F	ield		Туре	F	Reset	Des	cription	1						
	11:9	F	PGA[2:0]		R/W	2	2h		se bits s tion on t : FSR = : FSR =	et the F the ADS ±6.144 ±4.096 ±2.048 ±1.024 ±0.512 ±0.256 ±0.256	V ⁽¹⁾ V ⁽¹⁾ V (defa V V V V	ne progr	-		mplifier	. T
Configur Register		1	1	0	0	0	0	1								
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	





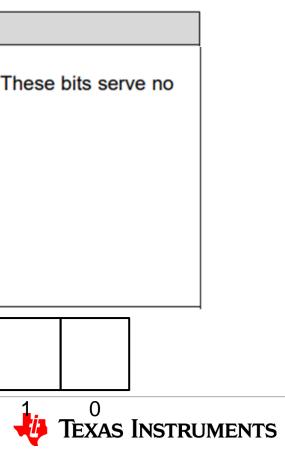
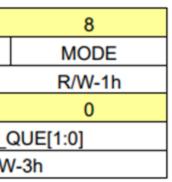


Figure 36. Config Register

15	14	13	12	11	10	9
OS		MUX[2:0]			PGA[2:0]	
R/W-1h		R/W-0h			R/W-2h	
7	6	5	4	3	2	1
	DR[2:0]		COMP_MODE	COMP_POL	COMP_LAT	COMP_C
	R/W-4h		R/W-0h	R/W-0h	R/W-0h	R/M
•						

_								_	-			-				
	Bit	F	ield		Туре	F	Reset	Des	cription	1						
	8	N	IODE		R/W		lh		ice ope bit cont		node operatir	ng mode) .			
	0	IV						0 : Continuous-conversion mode 1 : Single-shot mode or power-down state (default)								
Configura Register	ation	1	1	0	0	0	0	1	1							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	





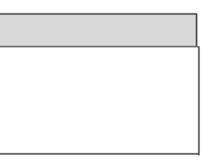




Figure 36. Config Register

R/W-1h R/W-0h R/W-2h 7 6 5 4 3 2 1 DR[2:0] COMP_MODE COMP_POL COMP_LAT COMP_	15	14	13	12	11	10	9
7 6 5 4 3 2 1 DR[2:0] COMP_MODE COMP_POL COMP_LAT COMP_	OS		MUX[2:0]			PGA[2:0]	
	R/W-1h		R/W-0h			R/W-2h	
	7	6	5	4	3	2	1
		DR[2:0]		COMP_MODE	COMP_POL	COMP_LAT	COMP_C
		R/W-4h		R/W-0h	R/W-0h	R/W-0h	R/W

Table 8. Config Register Field Descriptions

	Bit	Field	1		Туре	1	Reset	Des	cription	I						
	7:5	DR[2:0]		R/W 4h		4h	Data rate These bits control the data rate setting. 000 : 8 SPS 001 : 16 SPS 010 : 32 SPS 011 : 64 SPS 100 : 128 SPS (default) 101 : 250 SPS 110 : 475 SPS 111 : 860 SPS									
Configur Register		1	1	0	0	0	0	1	1	1	1	1				
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	



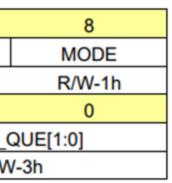




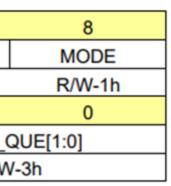


Figure 36. Config Register

-							
	15	14	13	12	11	10	9
[OS		MUX[2:0]			PGA[2:0]	
	R/W-1h		R/W-0h			R/W-2h	
	7	6	5	4	3	2	1
		DR[2:0]		COMP_MODE	COMP_POL	COMP_LAT	COMP_C
I		R/W-4h		R/W-0h	R/W-0h	R/W-0h	R/W

	Bit	Fie	eld		Туре		Reset	Des	cription	n						
	1:0	co	COMP_QUE[1:0]		R/W 3h		Comparator queue and disable (ADS1114 and ADS1115 or These bits perform two functions. When set to 11, the compara the ALERT/RDY pin is set to a high-impedance state. When set value, the ALERT/RDY pin and the comparator function are en value determines the number of successive conversions excee lower threshold required before asserting the ALERT/RDY pin. no function on the ADS1113. 00 : Assert after one conversion 01 : Assert after two conversions 10 : Assert after four conversions									
								11 :	Disable	compa	rator and	d set AL	ERT/RD)Y pin to	o high-in	npe
Configur Register		1	1	0	0	0	0	1	1	1	1	1	0	0	0	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	





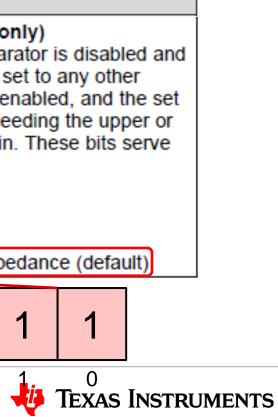


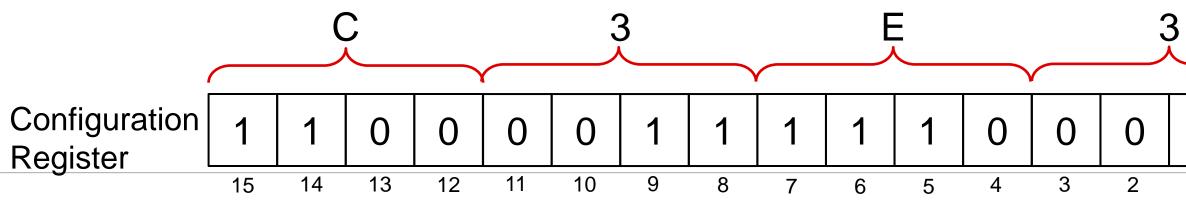
Figure 36. Config Register

_							
	15	14	13	12	11	10	9
	OS		MUX[2:0]			PGA[2:0]	
	R/W-1h		R/W-0h			R/W-2h	
	7	6	5	4	3	2	1
		DR[2:0]		COMP_MODE	COMP_POL	COMP_LAT	COMP_C
		R/W-4h		R/W-0h	R/W-0h	R/W-0h	R/W

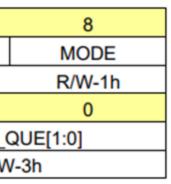
Table 8. Config Register Field Descriptions

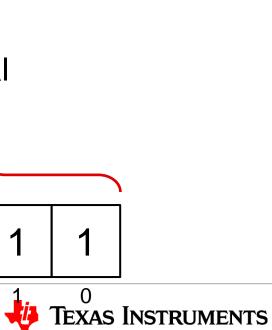
Bit	Field	Туре	Reset	Description
-----	-------	------	-------	-------------

Configuration Register can also be written as C3E3 in hexadecimal









13

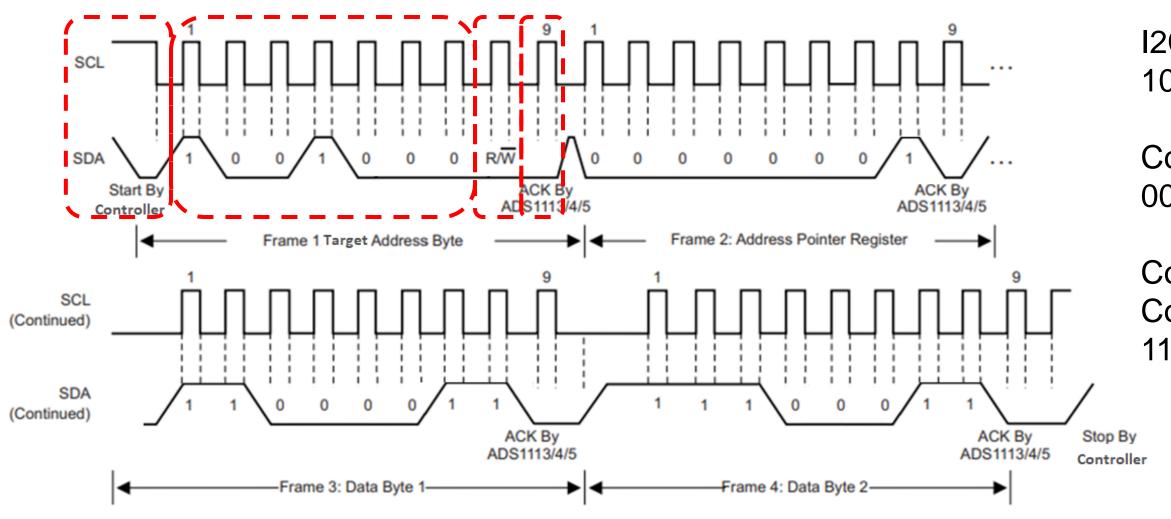


Figure 31. Timing Diagram for Writing to ADS111x

START, Address 48h, Write to device, ACK by ADS1115

I2C Address: 100 1000

Configuration Pointer: 0000 0001



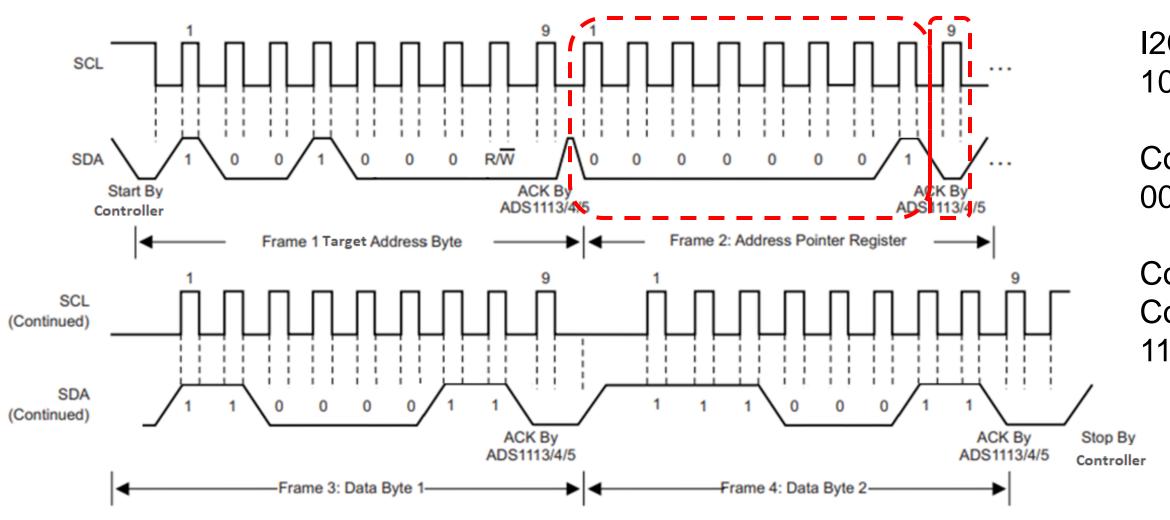


Figure 31. Timing Diagram for Writing to ADS111x

Send 01h to device for configuration register, ACK by ADS1115

I2C Address: 100 1000

Configuration Pointer: 0000 0001



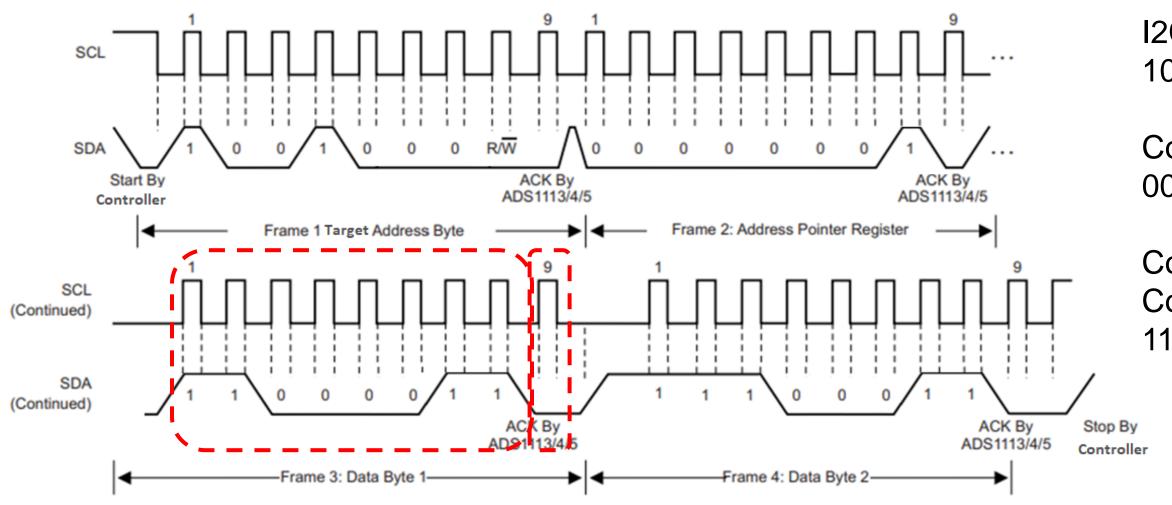


Figure 31. Timing Diagram for Writing to ADS111x

Send first configuration byte to device C3h, ACK by ADS1115

I2C Address: 100 1000

Configuration Pointer: 0000 0001





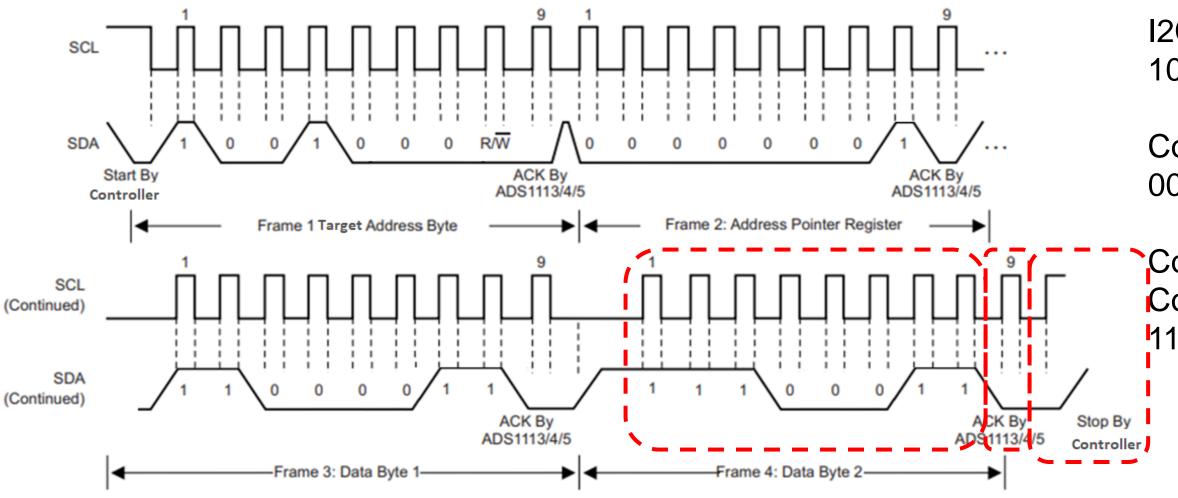


Figure 31. Timing Diagram for Writing to ADS111x

Send second configuration byte to device E3h, ACK by ADS1115, STOP

I2C Address: 100 1000

Configuration Pointer: 0000 0001



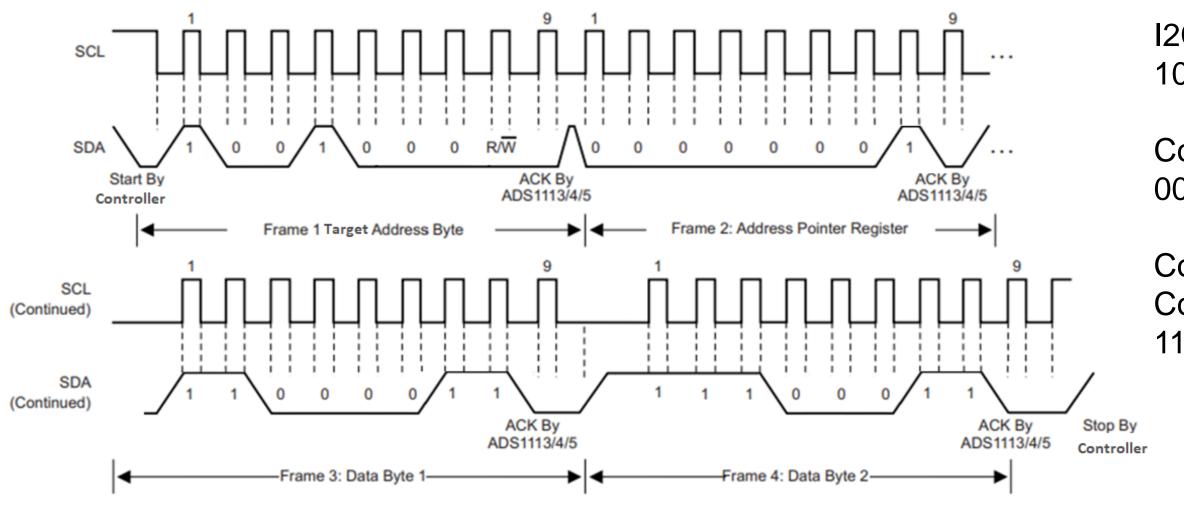


Figure 31. Timing Diagram for Writing to ADS111x

I2C Address: 100 1000

Configuration Pointer: 0000 0001



I2C Example: Reading from the Conversion Register

Figure 35. Conversion Register

15	14	13	12	11	10	9
D15	D14	D13	D12	D11	D10	D9
R-0h						
7	6	5	4	3	2	1
D7	D6	D5	D4	D3	D2	D1
R-0h						

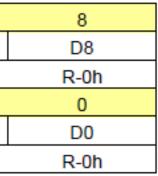
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Conversion Register Field Descriptions

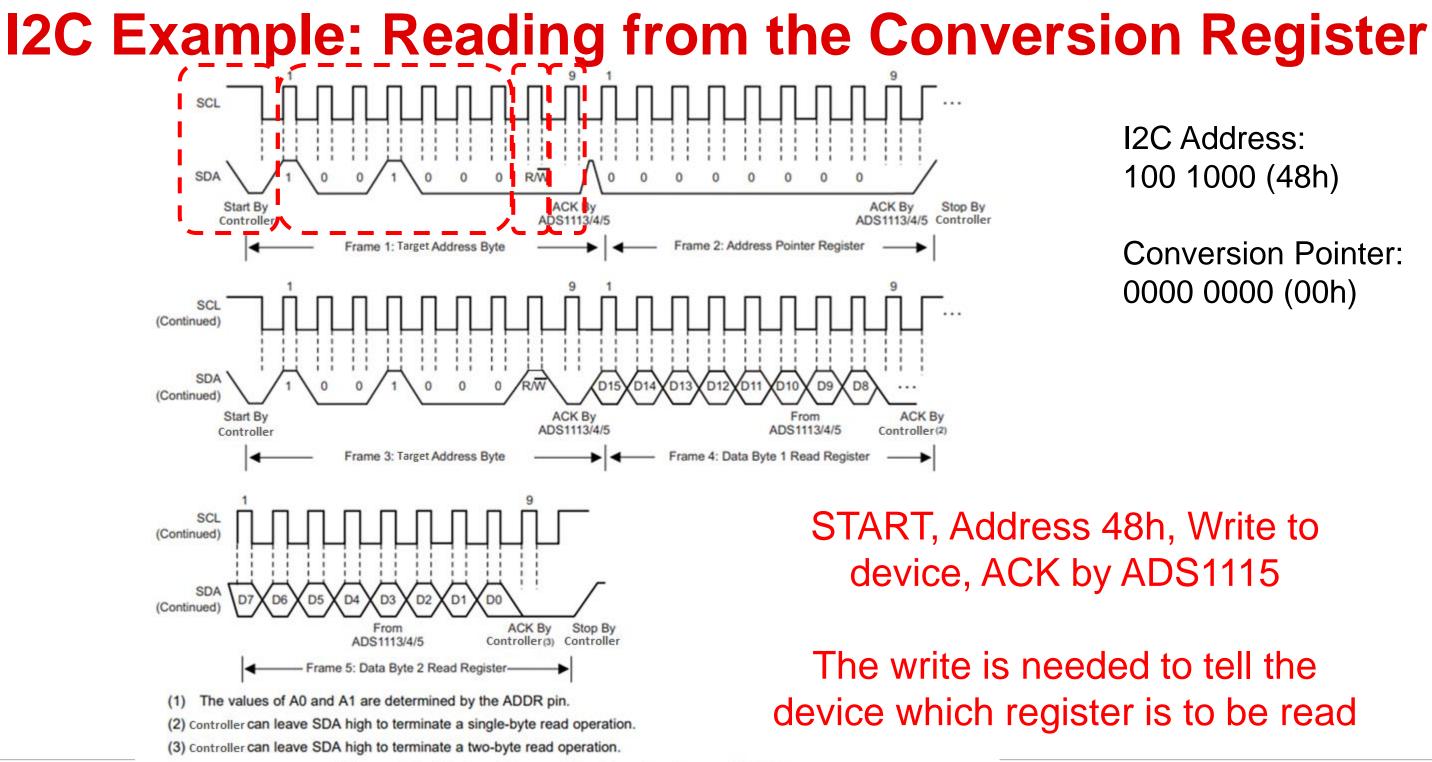
Bit	Field	Туре	Reset	Description
15:0	D[15:0]	R	0000h	16-bit conversion result

Conversion Register pointer: 0000 0000 Conversion data is 16 bits with MSB first



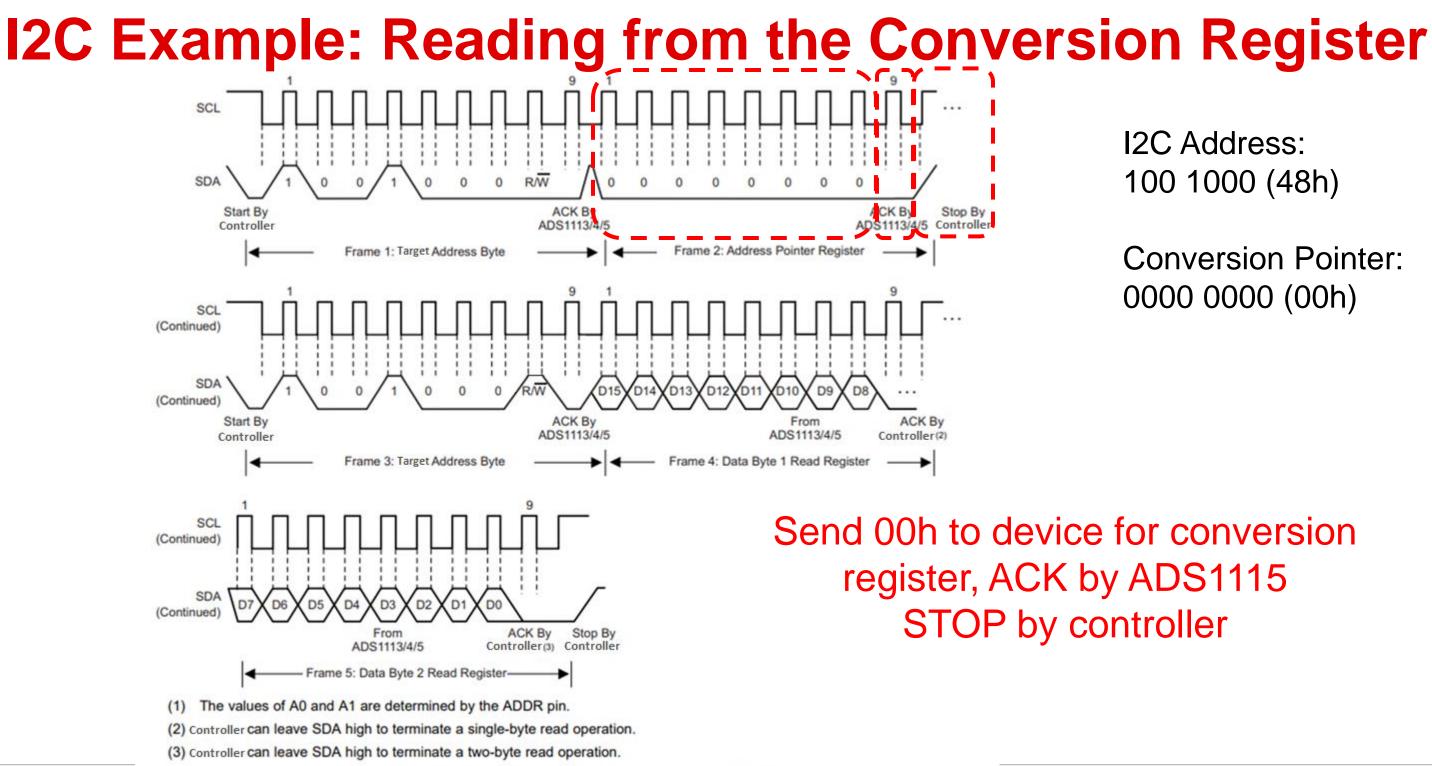






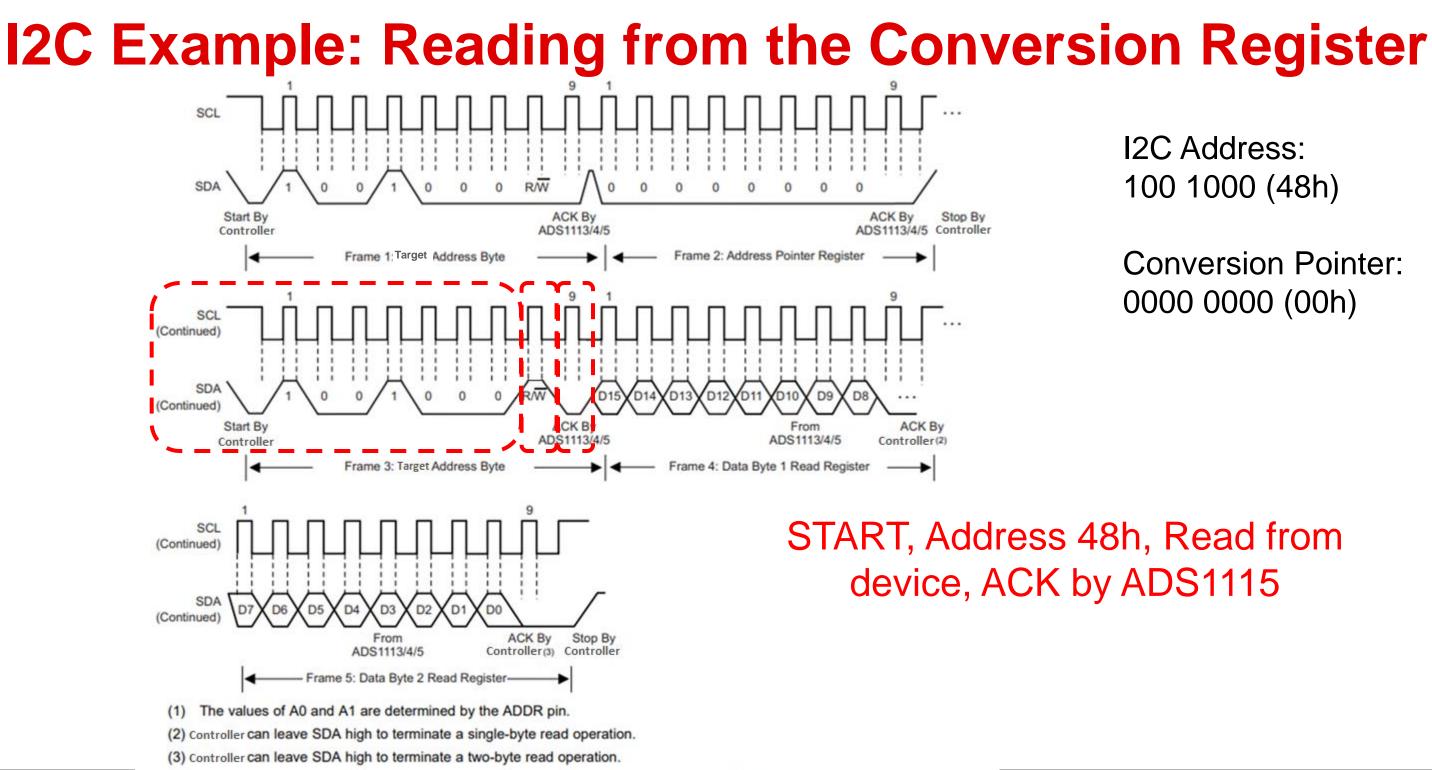
I2C Address: 100 1000 (48h)

Conversion Pointer: 0000 0000 (00h)



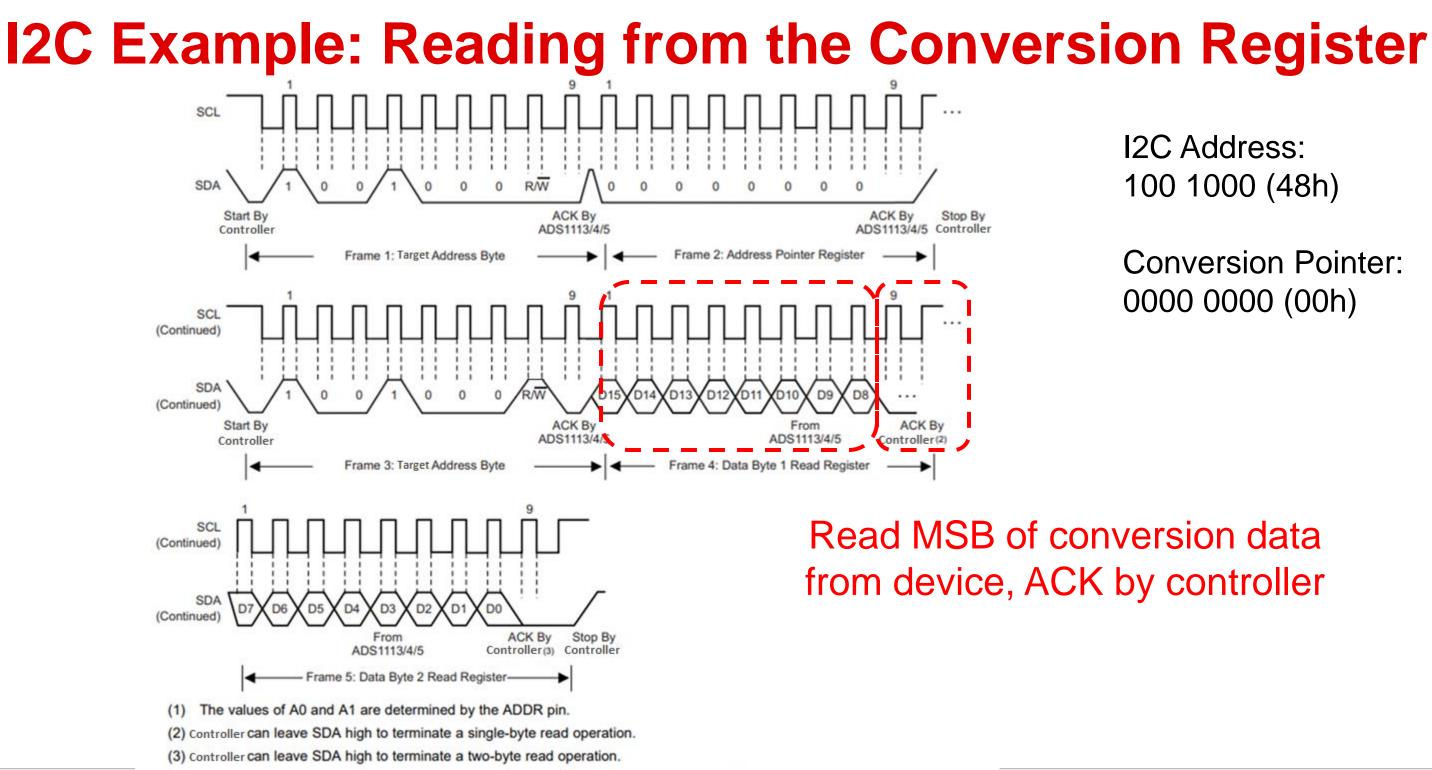
I2C Address: 100 1000 (48h)





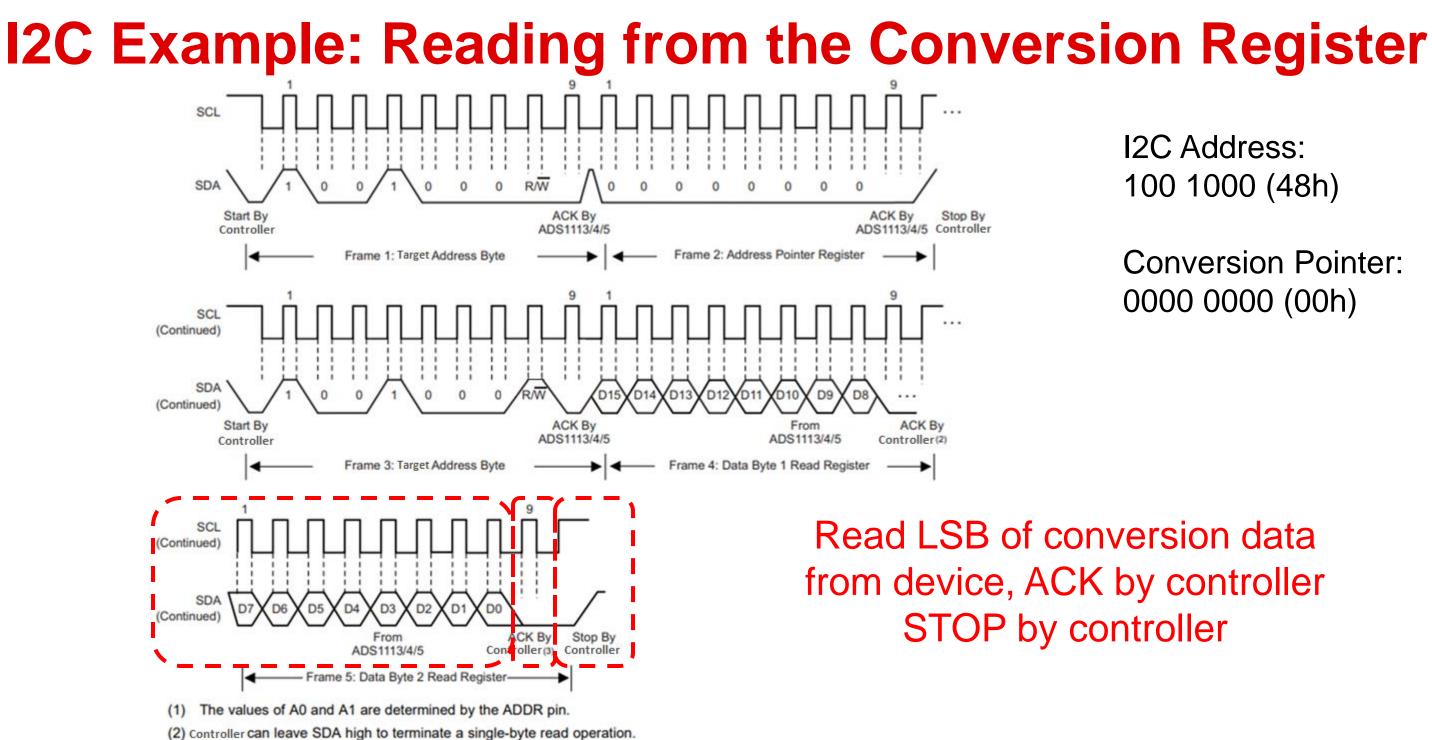
I2C Address: 100 1000 (48h)





I2C Address: 100 1000 (48h)





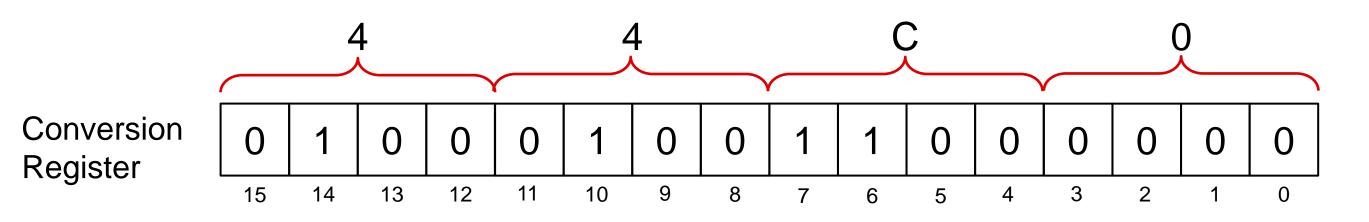
(3) Controller can leave SDA high to terminate a two-byte read operation.

Figure 30. Timing Diagram for Reading From ADS111x

I2C Address: 100 1000 (48h)



I2C Example: Reading from the Conversion Register



Example, PGA setting $\pm 4.096V$:

Conversion data register contents – 0100 0100 1100 0000 (44C0h)

In hex: 44C0h In decimal: 17600

Conversion result: Measurement = $(17600 / 2^{15}) \times 4.096V = 2.2 V$





Thanks for your time! Please try the quiz.



26

- 1. True/false: A write of the configuration register can be written with 16 consecutive bits, instead of breaking up the register into two, one-byte transfers.
 - a. True
 - b. False



- 1. True/false: A write of the configuration register can be written with 16 consecutive bits, instead of breaking up the register into two, one-byte transfers.
 - a. True





- 2. What is the I2C protocol byte order of a read from the ADS1115?
 - a. I2C address read, pointer address, data MSB, data LSB
 - I2C address write, pointer address, data MSB, data LSB b.
 - I2C address read, pointer address, I2C address read, data MSB, data LSB C.
 - d. I2C address write, pointer address, I2C address read, data MSB, data LSB



- 2. What is the I2C protocol byte order of a read from the ADS1115?
 - I2C address read, pointer address, data MSB, data LSB a.
 - I2C address write, pointer address, data MSB, data LSB b.
 - I2C address read, pointer address, I2C address read, data MSB, data LSB C.

I2C address write, pointer address, I2C address read, data MSB, data LSB



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Thanks for your time!







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Hello, and welcome to our in-depth look at communications with precision data converters. In this video, we describe I2C communication using a precision data converter as an example. We'll use an example to show how to write to and read from ADC using I2C.

I2C Example: ADS1115		
VDD VVDT VOLtage Reference AIN0 AIN1 AIN1 AIN2 AIN2 AIN3 Oscillator ADS1115	I2C Example Precision ADC wit data rates, and m I2C address is pin Device has four in ADDR Pin GND	configurable
GND	VDD	100 1001 (49h)
	SDA	100 1010 (4Ah)
	SCL	100 1011 (4Bh)
	ų	TEXAS INSTRUMENTS 2

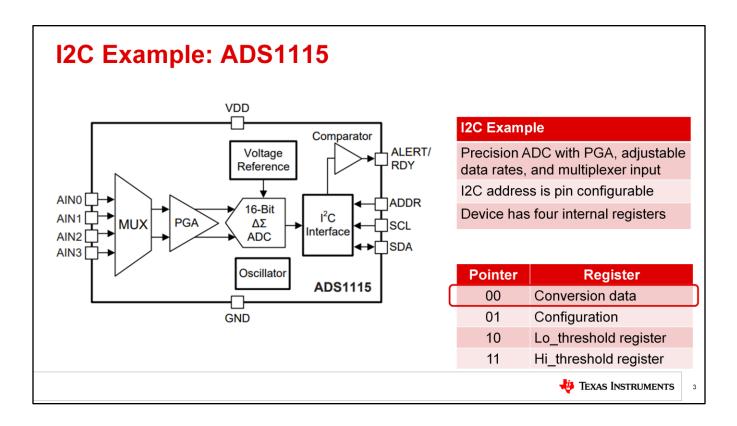
The ADS1115 is a 16-bit precision ADC. It uses an I2C interface and is capable of standard, fast, and high-speed modes. It has several settings that can be set through a configuration register, including the input range set by a programmable gain amplifier (or PGA), a variety of data rates, and a input multiplexer that can be set to make differential measurements, or single-ended measurements with respect to ground

The ADS1115 has an address pin labeled ADDR. This pin can be used to select one of four I2C addresses, meaning that four of these devices could be used on the same bus as long as the devices are programmed to different addresses. The I2C address used for the device depends on the ADDR pin connection.

With the ADDR pin connected to ground, the device has an I2C address of 48 in hex.

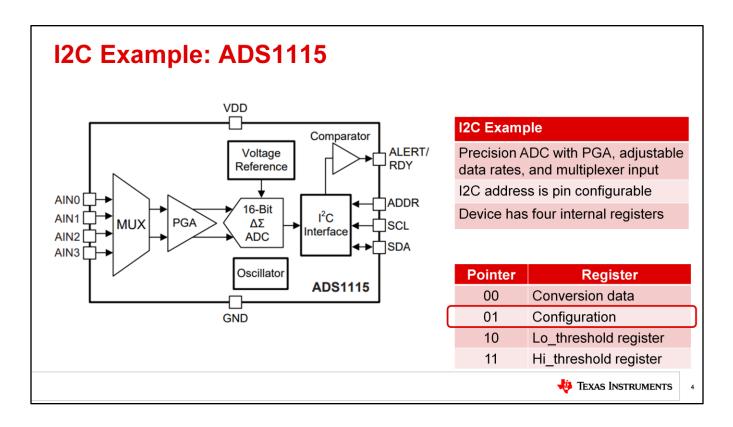
With the ADDR pin connected to VDD, SDA, or SCL, the device can be set to other addresses shown in the table.

For this example, we'll use the ADDR set to ground, so the address is 48 hex.

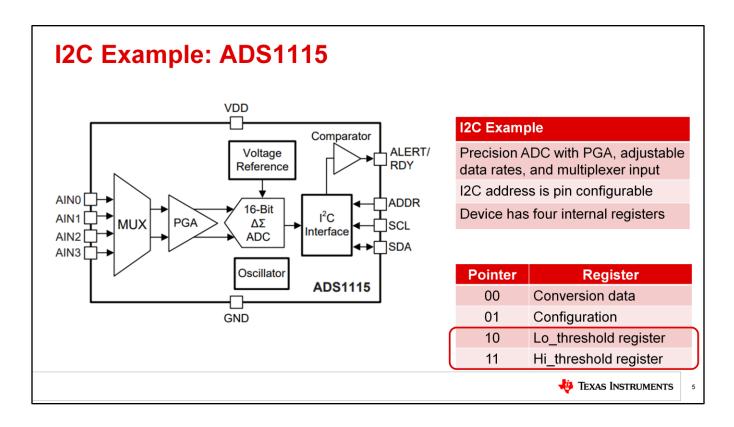


The ADS1115 has four internal registers, each addressed by an internal pointer register. The pointer register scheme in this example is a common method used in I2C devices with multiple registers.

The first register is the conversion data register. When the ADC completes a conversion, the ADC data is placed in this register and the controller device reads it out from here.



The second register is the configuration register. The controller device will write to this register to program the device and start a conversion. This register sets different aspects of the ADC conversion. It sets the programmable gain amplifier, the input channel, the data rate, and other modes of operation for the device. Later, we'll cover this register in depth, showing how to write to this register and configure the device.



The last two registers are the Lo_threshold register and the Hi_threshold register. These two registers are used to set thresholds for a digital comparator in the device. Once the conversion data goes beyond these thresholds, they can set an alert to the Alert/Ready pin. For this example, we won't configure the comparator and the thresholds.

For this example, we'll start with looking at the settings for the configuration register and using the I2C protocol to program the device.

15 14 13 12 11 10 9 8 OS MUX[2:0] PGA[2:0] MODE R/W-1h R/W-0h R/W-2h R/W-1h 7 6 5 4 3 2 1 0 DR[2:0] COMP_MODE COMP_POL COMP_LAT COMP_QUE[1:0] R/W-3h R/W-4h R/W-0h R/W-0h R/W-0h R/W-3h R/W-3h	C Example: Write to the Configuration Register												
OS MUX[2:0] PGA[2:0] MODE R/W-1h R/W-0h R/W-2h R/W-1h 7 6 5 4 3 2 1 0 DR[2:0] COMP_MODE COMP_POL COMP_LAT COMP_QUE[1:0]	15	14	13	-			9	8					
7 6 5 4 3 2 1 0 DR[2:0] COMP_MODE COMP_POL COMP_LAT COMP_QUE[1:0]	OS		MUX[2:0]			PGA[2:0]		MODE					
DR[2:0] COMP_MODE COMP_POL COMP_LAT COMP_QUE[1:0]	R/W-1h							R/W-1h					
	7	6	5	4	3	2	1	0					
R/W-4h R/W-0h R/W-0h R/W-3h		DR[2:0]		COMP_MODE	COMP_POL	COMP_LAT	COMP_	QUE[1:0]					
		R/W-4h		R/W-0h	R/W-0h	R/W-0h	R/V	V-3h					

The ADS1115 has a 16-bit configuration register. Writing to this register will program the configuration of the device and start a conversion. We'll discuss the settings for this configuration register and determine what to program into the device. Figure 36 from the datasheet shows the configuration register data fields. This shows the bit positions in the configuration register and what they are used for. Once we determine the all of the settings for the configuration register, we can use a I2C write to set the register.

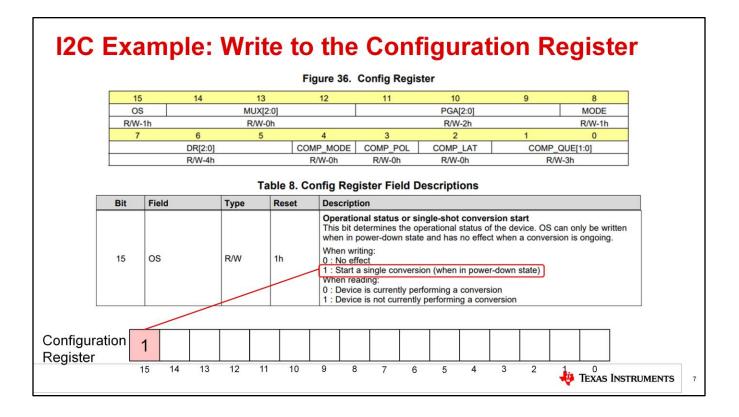
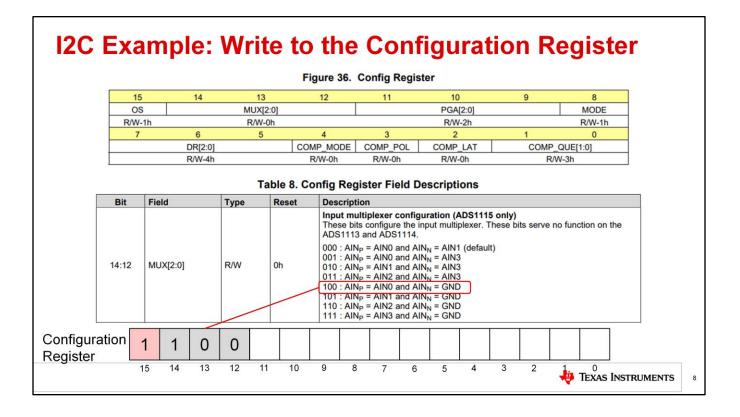


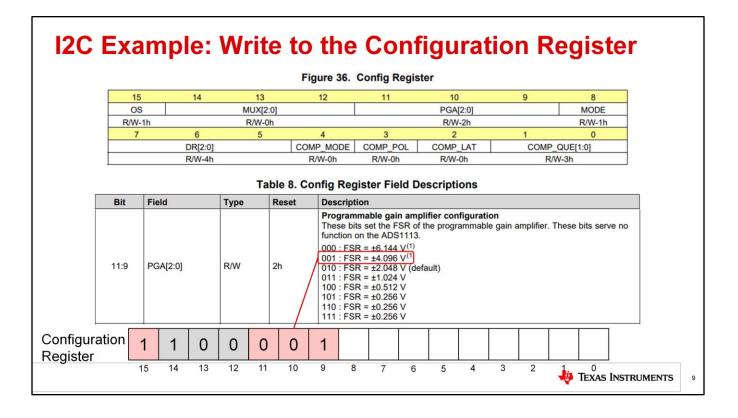
Table 8 in the datasheet shows the configuration register field descriptions, giving a detailed description of the bit setting. Starting with the most significant bit, bit 15 is the single-shot conversion start bit.

Setting bit 15 to 1 will start a single conversion.



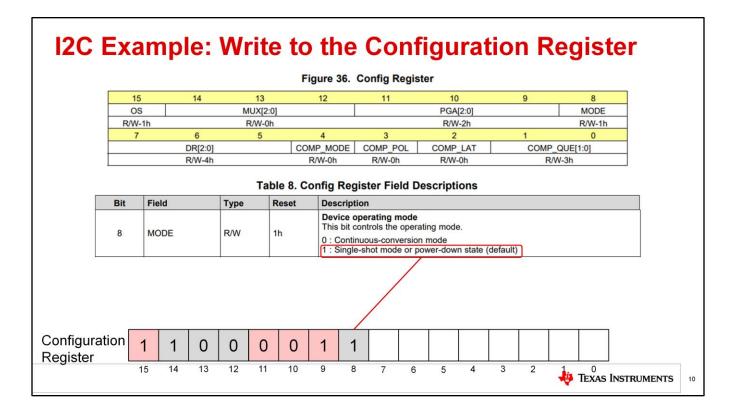
Bits 14 to 12 set the multiplexer setting of the device. For this example, we'll set the device to do a single-ended measurement from AINO with respect to ground. Using Table 8, we would set AINP to AINO and AINN to GND.

To do this, set bits 14 to 12 to be 100 in binary.



Bits 11 to 9 set the PGA setting of the device. This is the setting for the programmable gain amplifier. This sets the full-scale range of the input measurement, setting how large of an input signal can be measured by the ADC. Here, we set the ADC to measure a signal as large as plus and minus 4.096 Volts.

Set bits 11 to 9 to be 001 in binary.



Bit 8 sets the operating mode of the device. For this operation, we want to set the device to be in single-shot conversion mode

Set bit 8 to 1.

15 14 13 12 11 10 9 8 OS MUX[2:0] PGA[2:0] MODE RW-1h RW-0h RW-2h RW-1h 7 6 5 4 3 2 1 0 DR[2:0] COMP_MODE COMP_POL COMP_LAT COMP_QUE[1:0] RW-4h R/W-0h R/W-0h R/W-0h R/W-3h						Figure	36. Config	Register						
R/W-1h R/W-0h R/W-2h R/W-1h 7 6 5 4 3 2 1 0 DR[2:0] COMP_MODE COMP_POL COMP_LAT COMP_QUE[1:0] R/W-4h R/W-0h R/W-0h R/W-0h R/W-3h Table 8. Config Register Field Descriptions Bit Field Type Reset Description 000 : 8 SPS 001 : 16 SPS 001 : 16 SPS 001 : 32 SPS 001 : 32 SPS	15	5	14	1	3	12	11		10	9		8		
7 6 5 4 3 2 1 0 DR[2:0] COMP_MODE COMP_POL COMP_LAT COMP_QUE[1:0] R/W-4h R/W-0h R/W-0h R/W-0h R/W-0h Table 8. Config Register Field Descriptions Bit Field Type Reset Description 000 : 8 SPS 001 : 16 SPS 001 : 32 SPS 010 : 32 SPS	0	6		MUX	([2:0]				PGA[2:0]			MODE		
DR[2:0] COMP_MODE COMP_POL COMP_LAT COMP_QUE[1:0] R/W-4h R/W-0h R/W-0h R/W-0h R/W-3h Table 8. Config Register Field Descriptions Bit Field Type Reset Description 001 : 16 SPS 001 : 16 SPS 001 : 16 SPS	R/W	R/W-1h			V-0h				R/W-2h		R/M			
RW-4h RW-0h RW-0h RW-0h Table 8. Config Register Field Descriptions Bit Field Type Reset Description Data rate These bits control the data rate setting. 000 : 8 SPS 001 : 16 SPS 001 : 16 SPS 011 : 32 SPS	7			ŧ						· · ·				
Table 8. Config Register Field Descriptions Bit Field Type Reset Description Data rate These bits control the data rate setting. 000 : 8 SPS 001 : 16 SPS 001 : 16 SPS 000 : 3 SPS 001 : 16 SPS										C				
Bit Field Type Reset Description Data rate These bits control the data rate setting. 000 : 8 SPS 001 : 16 SPS 001 : 32 SPS			R/W-4h			R/W-0h	R/W-	Uh	R/W-0h		R/W-3h			
100 : 128 SPS (default) 101 : 250 SPS 110 : 475 SPS 111 : 860 SPS	7:5	DR[2:0]		R/W	4h	The 000 001 010 011 100 101 110	These bits control the data rate setting. 000 : 8 SPS 001 : 16 SPS 010 : 32 SPS 010 : 32 SPS 100 : 128 SPS (default) 101 : 250 SPS 110 : 475 SPS							
								-						
onfiguration 1 1 0 0 0 0 1 1 1 1 1 1	2000 C													

Bits 7 to 5 set the data rate for the ADC of the device. We can set this to the highest data rate of 860 samples per second.

Set bits 7 to 5 to 111.

I2C	Exa	n	npl	e:	Wı	ite	e t	0 1	the	Со	nf	igu	ra	tio	n F	Seč	gis	ter		
								Figu	re 36. (Config F	Regist	er								
	15	5		14		13		12	2	11		10)		9		8			
	0	5			M	UX[2:	0]					PGA	[2:0]				MODE			
	R/W	R/W-1h		R/W-0h		1			R/W-2h		/-2h	R/W-1h		h						
	7			6		5		4		3		2		-	1		0			
	-	DR[2:0]				COMP_MODE R/W-0h			COMP_P		COMP			COMP_QUE[1:0]						
			ŀ	R/W-4h				R/W	-un	R/W-0	1	R/W	-01		1	R/W-3h				
_						Tal	ole 8.	Conf	ig Regi	ster Fie	d De	escripti	ions							
	Bit	Fie	ld		Туре		Reset	0	Descriptio	on										
	1:0	co	MP_QU	JE[1:0]	Comparator queue and disable (ADS11 These bits perform two functions. When se the ALERT/RDY pin is set to a high-imped value, the ALERT/RDY pin and the compa value determines the number of successiv							Vhen se -impeda compar ccessive erting th	t to 11, 1 ance sta rator fun e conver he ALEF	the com te. Whe ction are sions ex RT/RDY	parator n set to e enable cceedin pin. The	any othed, and g the up ese bits	her the set oper or serve			
Configura Register	ation	1	1	0	0	0	0	1	1 1	1	1	1	0	0	0	1	1			
. logiotor	6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 Texas	5 Instr	UMENTS	12

The last five bits from 4 down to 0 are all used for the digital comparator for this device. We won't use the digital comparator here, so we'll disable this setting with the last two bits of the register and set the remaining bits to their default setting.

Set bits 4 to 0 to 00011.

	слани	Jie. V	rite	to the	Conf	igurat	ion Re	egister
				Figure 36.	Config Regis	ter		
	15	14	13	12	11	10	9	8
	OS		MUX[2:0]			PGA[2:0]		MODE
	R/W-1h		R/W-0h			R/W-2h		R/W-1h
	7	6	5	4	3	2	1	0
		DR[2:0]		COMP_MODE	COMP_POL	COMP_LAT	COMP_C	
	L	R/W-4h		R/W-0h	R/W-0h	R/W-0h	R/M	-011
г				8. Config Reg		escriptions		
L	Bit Field	Ту	pe Res	et Descript	ion			
	Con	figuration I	Register	can also be	e written as	s C3E3 in h	exadecima	
Configura Register		figuration I	~	can also be	e written as	s C3E3 in he	exadecima 3 0 0	1 1

Now we have the complete configuration register setting for the ADS1115. We'll use these bits for the write to the register. This register can also be represented in hexadecimal as C3E3.

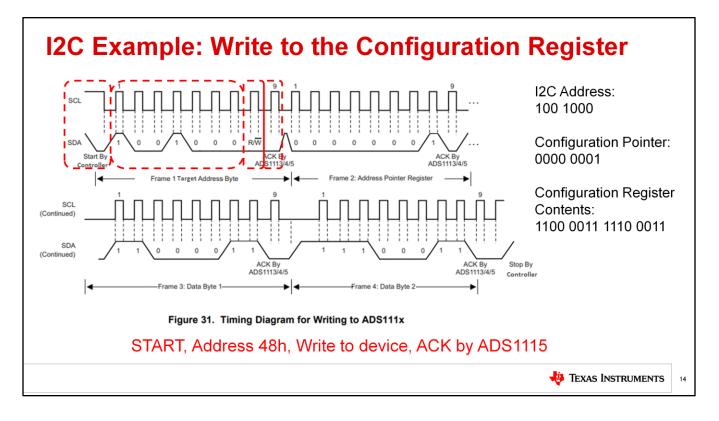


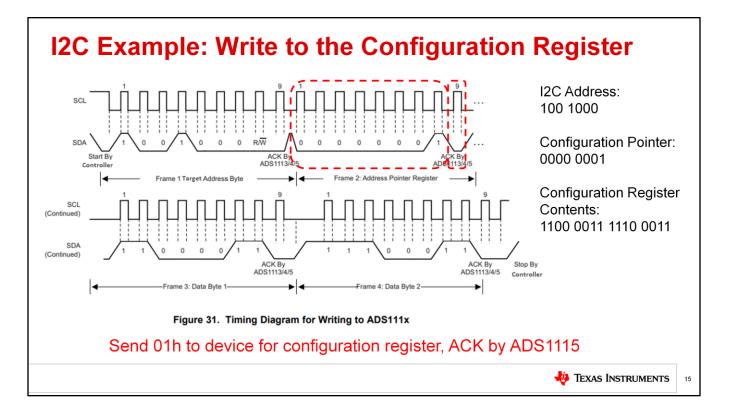
Figure 31 in the ADS1115 datasheet shows a generic diagram for writing to the device. The figure has been altered to show the exact bit transactions sent to the device. We'll use the settings that we've previously discussed to show exactly what we need to write to the configuration register. For reference, we'll put up the data we need on the right side of the slide.

First, the I2C write starts with a START Condition. SDA is pulled low, and then SCL is pulled low.

Then we write the I2C address. With the ADDR pin connected to ground, we use an address of 100 1000 (or 48 in hex).

The Read/Write bit is then set low, indicating that we want to write to the device.

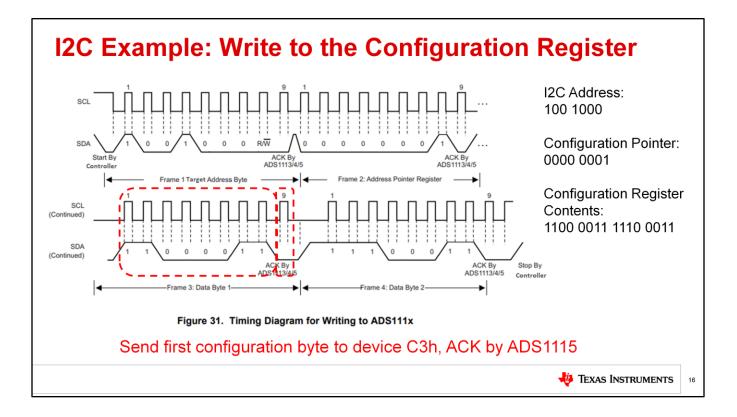
After the completion of the address frame, the ADS1115 should acknowledge the address by pulling down the SDA for the last bit of the address frame. The controller sends out the address and read/write information to all of the slaves on the bus. If a target has a matching address, they will acknowledge to let the controller know that this is a valid address and they are ready to receive information. This ACK lets the controller know that the target device is ready for communication.



After we've indicated that we want to write to the ADS1115, we need to tell the device that we want to write to the configuration register.

The second byte is the register pointer for the configuration register. Here, we send 0000 0001 to the ADS1115.

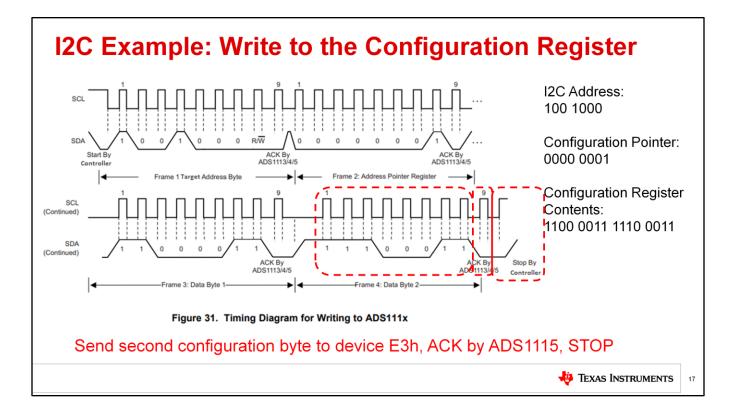
As a response, the ADS1115 pulls down on SDA for an ACK. Again, the target device is letting the controller know it has received the address pointer data.



Now we start to send in the configuration register data one byte at a time.

For this byte, we send in the first byte of the configuration register. Here, we send 1100 0011 to the ADS1115.

The ADS1115 ACKs the first byte and pulls down on SDA for the last bit.

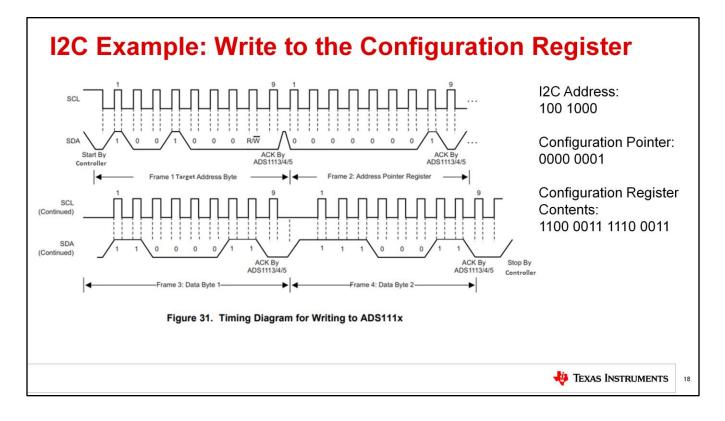


Finally, we send in the last byte of the configuration register.

Here, we send 1110 0011 to the ADS1115.

The ADS1115 ACKs the first byte and pulls down on SDA for the last bit.

At the end, the controller releases the bus by issuing a STOP condition. SCL is released high and then SDA is released high.



Putting it all together, Figure 31 now looks like this: [Click] Here you have the same diagram with all the proper bit settings for all frames. Figure 31 in the datasheet is very useful when debugging communications. You could plot the I2C communication with an oscilloscope, and compare this figure with the plot.

			Figu	ire 35. Conv	version Regis	ter		
15	14		13	12	11	10	9	8
D1	5 D14	(013	D12	D11	D10	D9	D8
R-0	h R-0h	F	0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6		5	4	3	2	1	0
D7	D6		D5	D4	D3	D2	D1	D0
R-0	h R-Oh	F	≀-0h	R-0h	R-0h	R-0h	R-0h	R-0h
Bit	Field				gister Field [Descriptions		
Bit	Field	Туре	Reset	Descriptio	n	Descriptions		
Bit 15:0	Field D[15:0]			Descriptio	-	Descriptions		

The ADS1115 has a 16-bit ADC and therefore puts out 16bit data conversions. To get the ADC conversion data, you need to read from a conversion register. The conversion register address pointer is 0000 0000.

Figure 35 from the datasheet shows the conversion register data field and Table 8 in the datasheet shows the configuration register field description. Conversion data appears as a 16 bit result in binary two's complement. A positive full-scale input produces an output code of 7FFFh and a negative full-scale input produces an output code of 8000h.

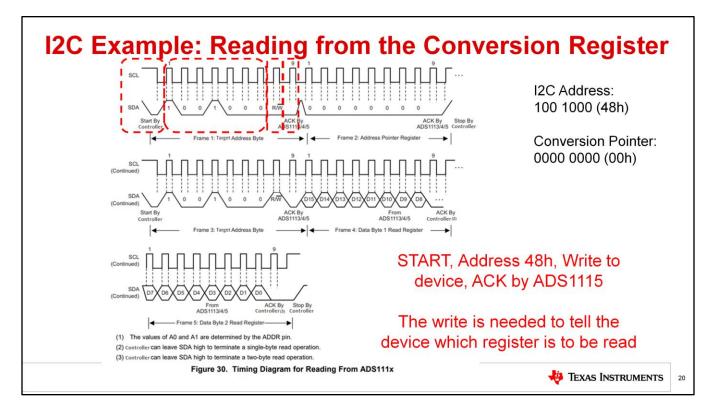


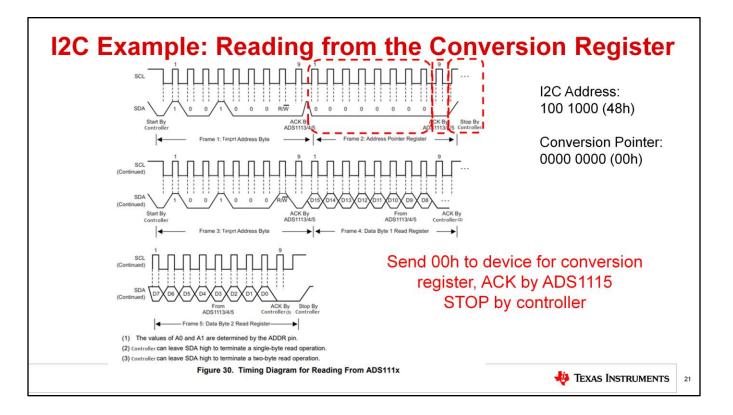
Figure 30 in the ADS1115 datasheet shows a generic diagram for reading from the device. Again, we'll use the settings that we've previously discussed to show exactly what we need to read from the conversion register. For reference, we'll put up the address and the register pointer that we need on the right side of the slide.

First, the I2C write starts with a START Condition. SDA is pulled low, and then SCL is pulled low.

Then we write the I2C address. With the ADDR pin connected to ground, we use an address of 100 1000 (or 48 in hex).

We need to tell the device which register we need to read from. For this, we need a *WRITE* to the device so that we can set up the read from the ADS1115. At this point, the Read/Write bit is then set low, indicating that we want to write to the device.

After the completion of the address frame, the ADS1115 acknowledges the address by pulling down the SDA for the last bit of the address frame.

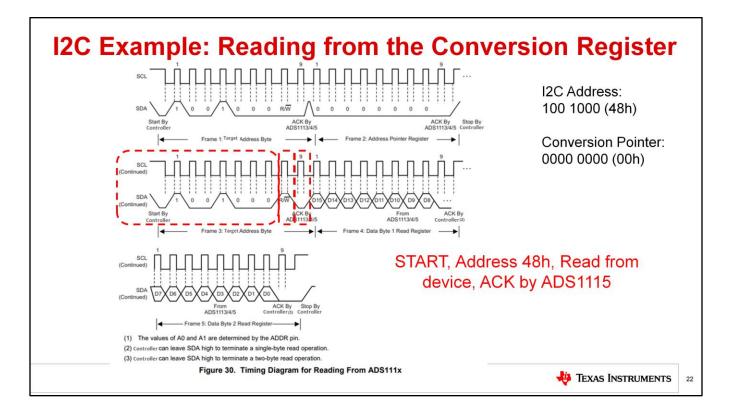


After we've indicated that we want to *WRITE* to the ADS1115, we need to tell the device that we want to access the configuration register.

The second byte is the register pointer for the configuration register. Here, we send 0000 0000 to the ADS1115.

As a response, the ADS1115 pulls down on SDA for an ACK.

Finally the controller issues a STOP to release the bus.

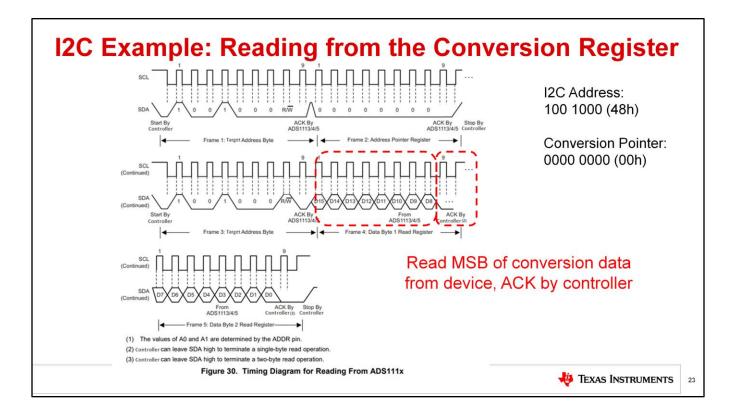


Now that we've told the device we want to access the conversion register, we follow up with the read from the conversion register.

We write the I2C address again.

Now, we need a *READ* from the device from the conversion register of the ADS1115. At this point, the Read/Write bit is then set high, indicating that we now want to read from the device.

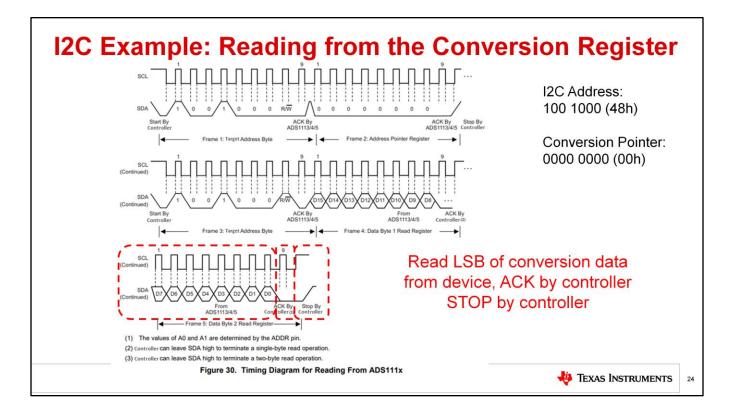
Again after the completion of the address frame, the ADS1115 should ACK the address.



Now, we can read the conversion register one byte at a time.

First you read the most significant byte.

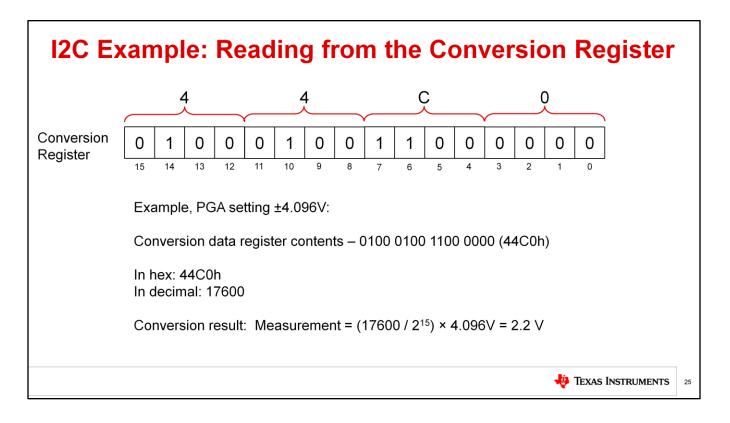
And as a response for reading the data, the controller device pulls down on SDA for an ACK. Because the target device is sending data, it is now the controller device that pulls down SDA for an ACK. This tells the target device that the data has been received by the controller device.



Then follows the read of the least significant byte.

An then another ACK from the controller.

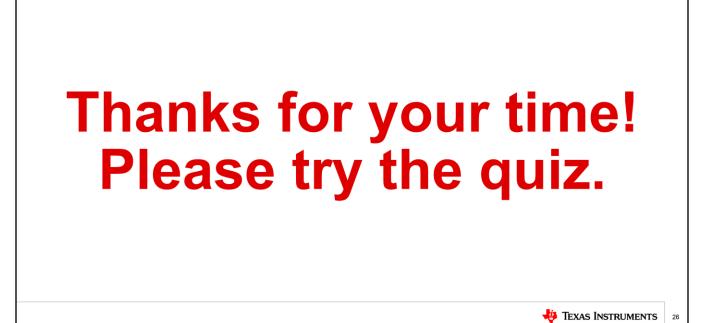
Finally, the controller sends a STOP to end the I2C communication.



Just to follow up with the conversion register result, let's use one last example with reading data and making the conversion.

Let's say you read out the data from the conversion register and it reads 44C0 in hex, or 17600 in decimal. This is the ADC output based on the input voltage from the measurement.

Using this value, you can convert the conversion register to a voltage for the ADC measurement. With a positive full scale range of 4.096V, you can convert this to a measured voltage. Here, the ADC is reporting 2.2V



That concludes this video – thank you for watching! Please try the quiz to check your understanding of this video's content.

Quiz: Basics of I2C: An I2C Example

- 1. True/false: A write of the configuration register can be written with 16 consecutive bits, instead of breaking up the register into two, one-byte transfers.
 - a. True
 - b. False

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Quiz: Basics of I2C: An I2C Example	
 True/false: A write of the configuration register can be written with 16 consecutive bits, instead of breaking up the register into two, one-byte transfers. a. True b. False 	
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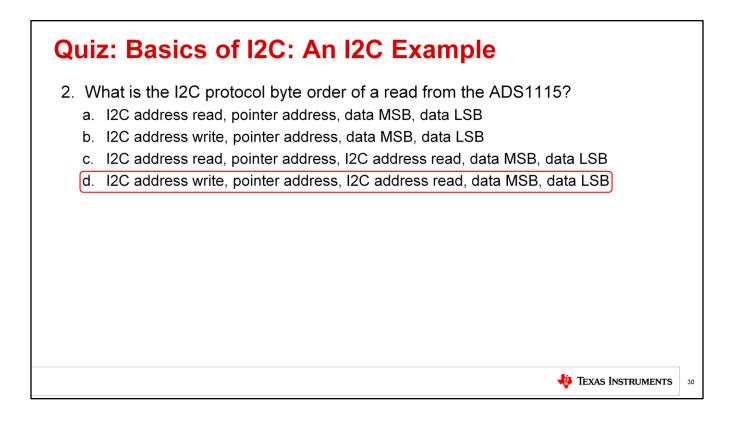
I2C transmissions come in single byte transmission frames. This is standardized and both controller devices and target devices know that the transmission will come in a set format.

Quiz: Basics of I2C: An I2C Example

- 2. What is the I2C protocol byte order of a read from the ADS1115?
 - a. I2C address read, pointer address, data MSB, data LSB
 - b. I2C address write, pointer address, data MSB, data LSB
 - c. I2C address read, pointer address, I2C address read, data MSB, data LSB
 - d. I2C address write, pointer address, I2C address read, data MSB, data LSB

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While, the objective of this sequence is to read the conversion register, we still need to tell the target device what register the controller wants to read from. Notice that we first write to the pointer register, before we can read that register.

Thanks for your ti

