Driving SAR ADC Without Amplifiers

TI Precision Labs – ADCs

Presented by Art Kay

Prepared by Keith Nicholas, Cynthia Sosa, Art Kay

Find sampling rate: ADC without buffer amplifier

General Equations for Sampling Rate given a source impedance Rin to achieve 1/2 LSB settling accuracy

$$C_{filt} = 20 \cdot C_{sh}$$

$$t_{AcqMin} = R_{in} \cdot (C_{filt} + C_{sh}) \cdot ln\left(\frac{2 \cdot 2^N \cdot C_{sh}}{C_{filt} + C_{sh}}\right)$$

$$f_s = \frac{1}{t_{AcqMin} + t_{ConvMax}}$$

ADS8860 Example

$V_{fs} := 5\ V \qquad R_{in} := 1\ k\Omega$

$C_{sh} := 55\ pF \qquad t_{ConvMax} := 710\ ns \qquad N := 16$

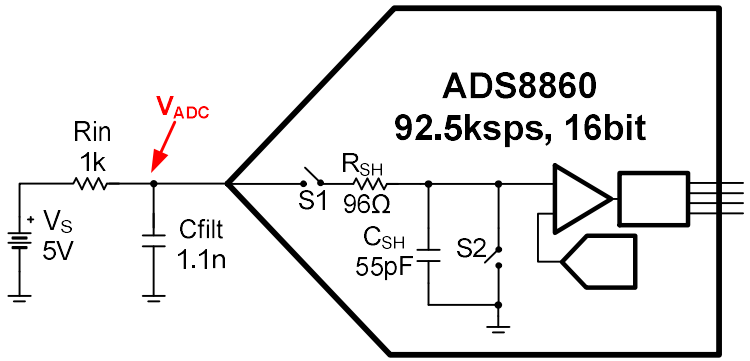
$C_{filt} := 20 \cdot C_{sh} = 1.1\ nF$

$$t_{AcqMin} := R_{in} \cdot (C_{filt} + C_{sh}) \cdot \ln\left(\frac{2 \cdot 2^N \cdot C_{sh}}{C_{filt} + C_{sh}}\right) = 10.094\ \mu s$$

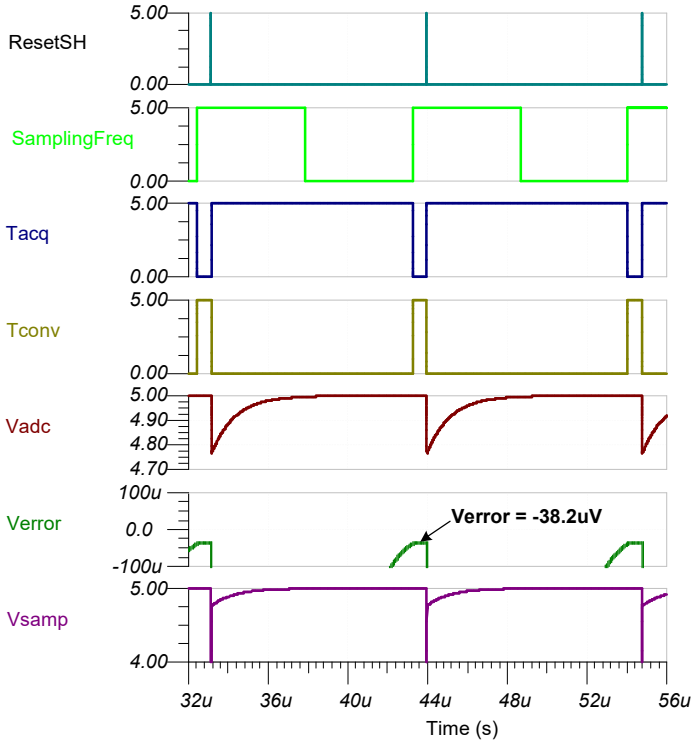
$$f_s := \frac{1}{t_{AcqMin} + t_{ConvMax}} = 92.562\ kHz$$

$$Half\_LSB := \frac{V_{fs}}{2 \cdot 2^N} = 38.147\ \mu V$$

$$f_c := \frac{1}{2\ \pi \cdot R_{in} \cdot C_{filt}} = 144.686\ kHz$$



- This procedure assumes that Rin is known
- Rin may be the source impedance of the sensor.
- Targeted settling error of 1/2LSB
- Simulated settling error approximately 1/2LSB (1/2LSB = 38.1µV, Sim = 38.2µV)



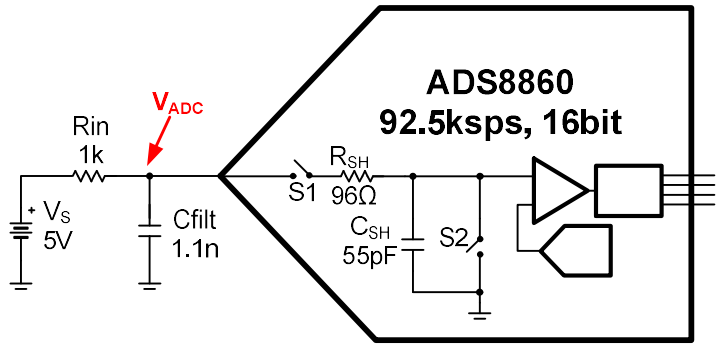
Initial start up time

Initial Settling of RC filter

$N = 16 \quad R_{in} := 1\ k\Omega$

$C_{sh} := 15\ pF \quad C_{filt} := 1.1\ nF$

$t_{settling} := R_{in} \cdot (C_{sh} + C_{filt}) \cdot \ln(2^N) = 9.274\ \mu s$



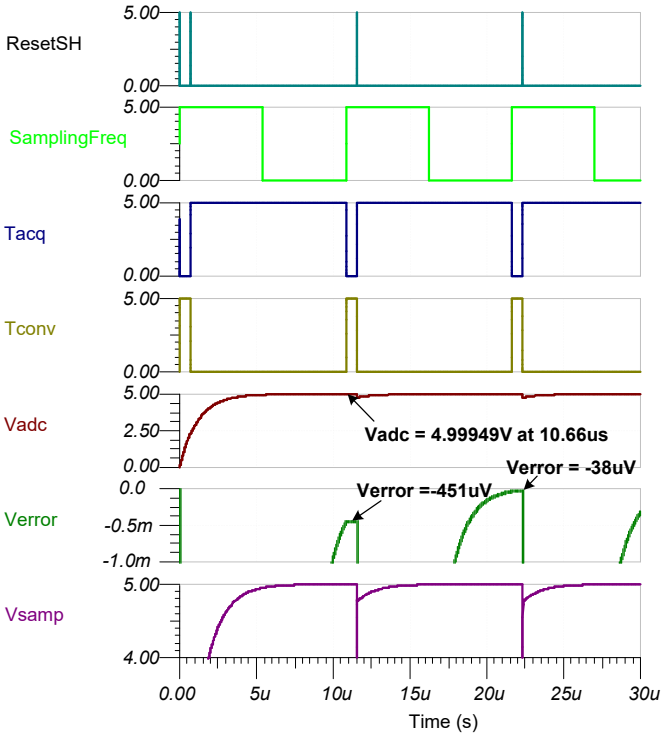


Table 38: Time required to settle to a specified conversion accuracy

Accuracy in bits (N)	Settling time in time constants (N_{TC})	Accuracy in bits (N)	Settling time in time constants (N_{TC})
8	5.5	17	11.78
9	6.24	18	12.48
10	6.93	19	13.17
11	7.62	20	13.86
12	8.32	21	14.56
13	9.01	22	15.25
14	9.70	23	15.94
15	10.40	24	16.64
16	11.04	25	17.33

$N_{TC} = \ln(2^N)$ (201)

- The results on the previous slide assume that the input RC filter is settled.
- The initial settling time requirement can be calculated using the equations shown.
- This equation assumes settling for a resolution requirement.
- The simulation shows that the first sample has worse error due to the start-up charging of the input RC filter

Find input source impedance for sampling rate

ADS7047 Example: Find a voltage divider that will settle with 100kHz sampling rate

$C_{sh} := 16\ pF \quad t_{ConvMax} := 250\ ns$

$f_s := 100\ kHz \quad V_{in} := 10\ V \quad V_{adc} := 3.6\ V$

$C_{filt} := 20 \cdot C_{sh} = 320\ pF \quad N := 12$

$t_{AcqMin} := \frac{1}{f_s} - t_{ConvMax} = 9.75\ \mu s$

$R_{in} := \frac{t_{AcqMin}}{(C_{filt}+C_{sh}) \cdot \ln\left(\frac{2 \cdot 2^N \cdot C_{sh}}{C_{filt}+C_{sh}}\right)} = 4.864\ k\Omega$

$R_{in} = \frac{R_1 \cdot R_2}{R_1+R_2} = 4.864\ k\Omega$

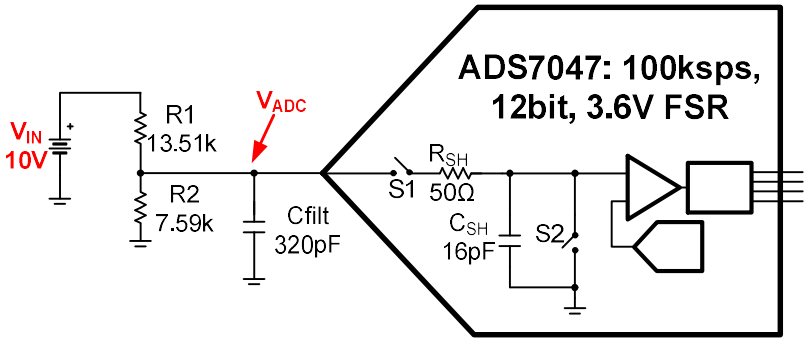
$V_{adc} = \frac{R_2 \cdot 10\ V}{R_1+R_2} = 3.6\ V$

Solve for R1, R2

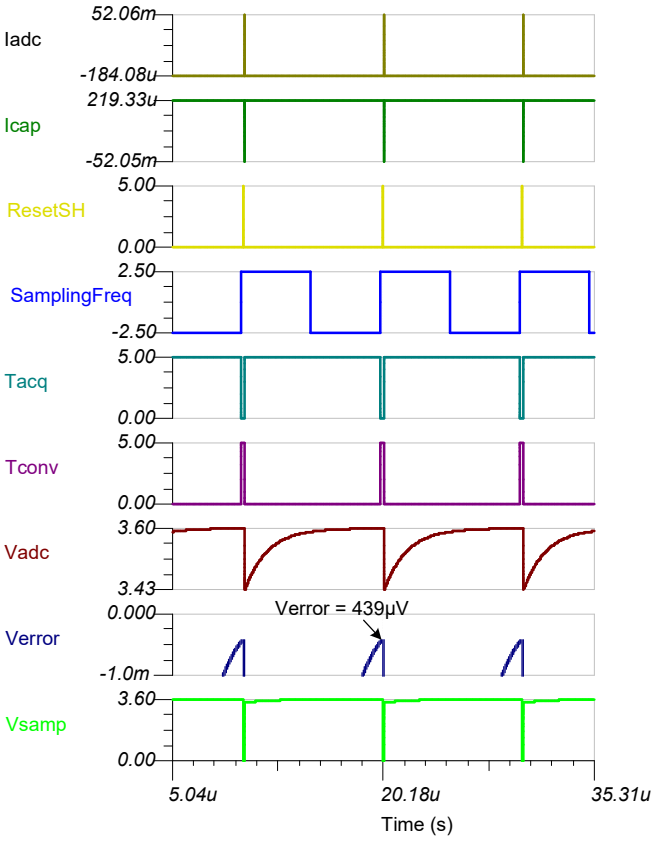
$R_2 := \left(\frac{V_{in}}{V_{in}-V_{adc}}\right) \cdot R_{in} = 7.599\ k\Omega$

$R_1 := \left(\frac{V_{in}-V_{adc}}{V_{adc}}\right) \cdot R_2 = 13.51\ k\Omega$

$Half\_LSB := \frac{3.6\ V}{2 \cdot 2^N} = 439.453\ \mu V$



- This procedure assumes a desired sampling rate, and solves for the required source impedance (Rin)
- The source impedance for the voltage divider is the parallel combination of R1 and R2
- Settling Error matches the expected error (1/2LSB = 439µV, Sim = 439µV)



Periodic single-shot conversions

General Equations for recovery period for 1/2 LSB settling on single shot conversion.

$$C_{filt} = 2 \cdot 2^N \cdot C_{sh}$$

$$t_1 = R_{in} \cdot (C_{filt} + C_{sh}) \cdot ln(2)$$

$$t_{recovery} = t_1 + t_{ConvMax}$$

ADS7042 Example

$$R_{in} := 100\ k\Omega \quad C_{sh} := 15\ pF$$

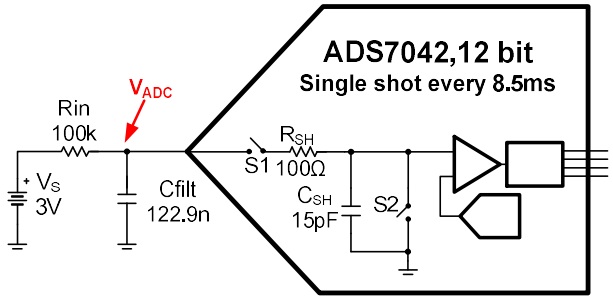
$$t_{ConvMax} := 800\ ns \quad N := 12$$

$$C_{filt} := 2 \cdot 2^N \cdot C_{sh} = 122.88\ nF$$

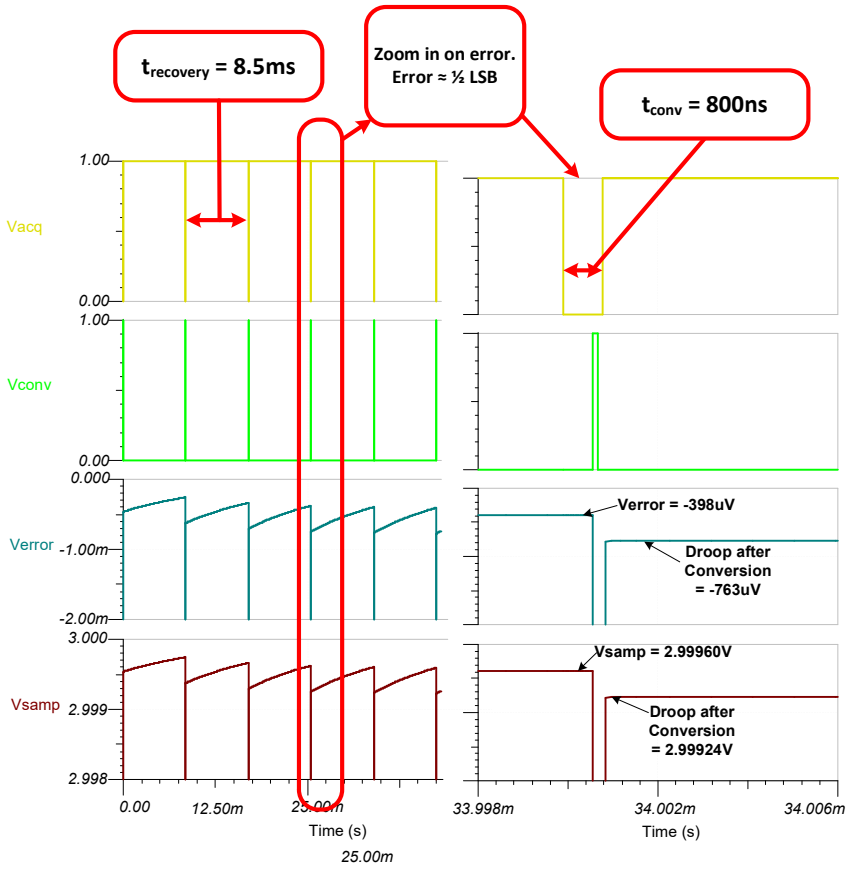
$$t_1 := R_{in} \cdot (C_{filt} + C_{sh}) \cdot \ln(2) = 8.518\ ms$$

$$t_{recovery} := t_1 + t_{ConvMax} = 8.519\ ms$$

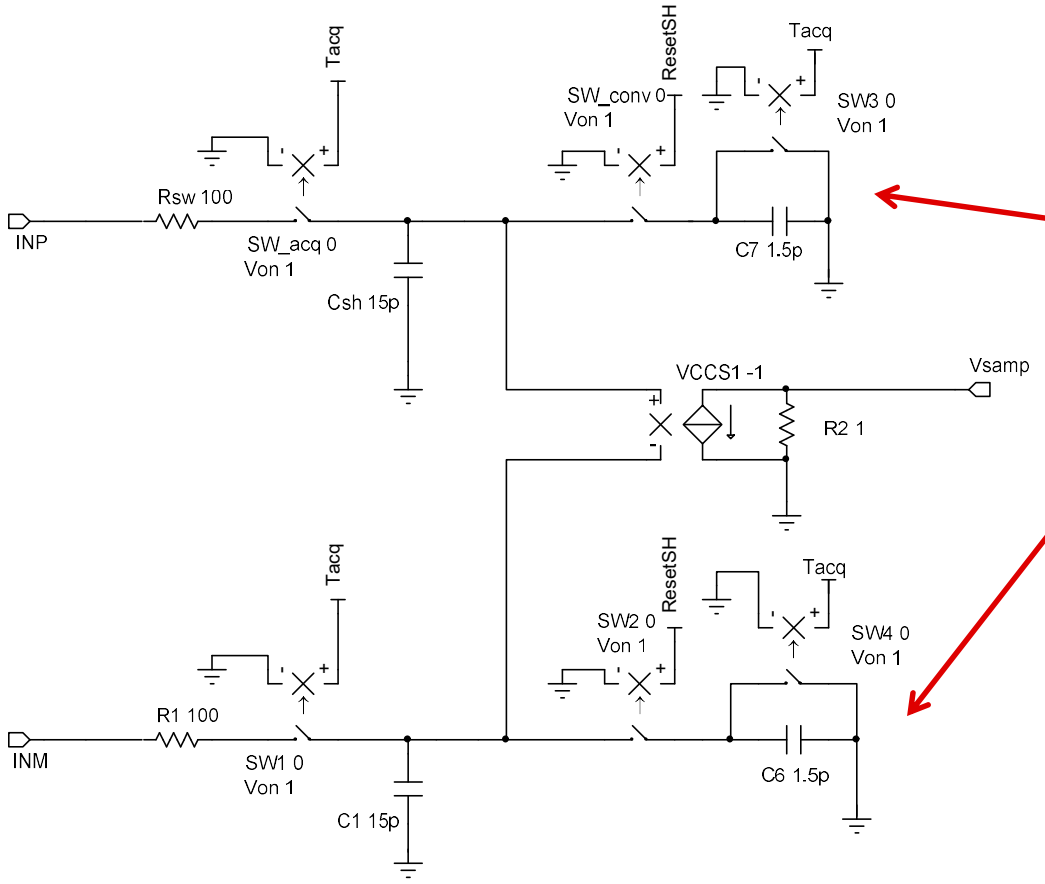
$$Half\_LSB := \frac{3\ V}{2 \cdot 2^{12}} = 366.211\ \mu V$$



- This procedure assumes a fast single-shot conversion is done periodically
- The capacitor is selected to so that error is 1 LSB at start of acquisition period
- The recovery time is set so that the error is ½ LSB at start of conversion.
- Simulated settling error approximately 1/2LSB (1/2LSB = 366µV, Sim = 398µV)



Is the sample and hold completely reset?



The reset capacitors deplete the charge on the sample and hold capacitor by 10% at end of conversion cycle. The old model reset to zero. Assuming the input signal is DC, the input capacitor looks like an effective capacitance of 1.5pF in this example.

Multiplexed inputs – Component selection

ADS8168 Example: Find a voltage divider that will settle with 100kHz sampling rate

$C_{sh} := 60\ pF \quad t_{ConvMax} := 600\ ns$

$N := 16 \quad C_{mux} := 13\ pF$

$f_s := 100\ kHz \quad V_{in} := 10\ V \quad V_{adc} := 4.8\ V$

$C_{filt} := 20 \cdot (C_{sh} + C_{mux}) = 1.46\ nF$

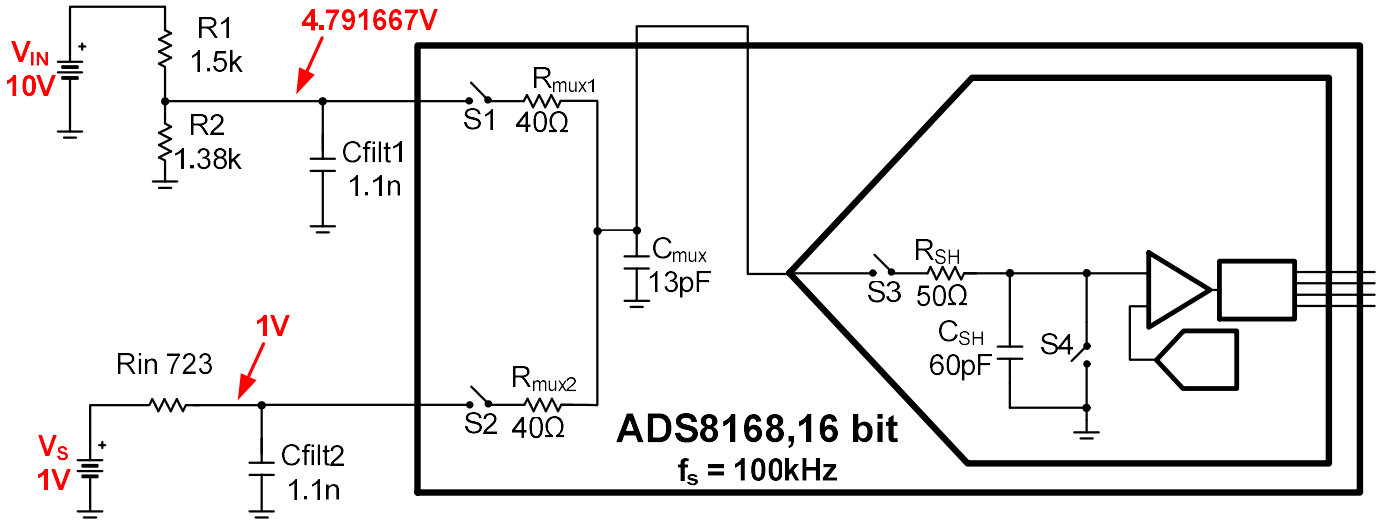
$t_{AcqMin} := \frac{1}{f_s} - t_{ConvMax} = 9.4\ \mu s$

$R_{in} := \frac{t_{AcqMin}}{(C_{filt} + C_{sh}) \cdot \ln\left(\frac{2 \cdot 2^N \cdot C_{sh}}{C_{filt} + C_{sh}}\right)} = 0.723\ k\Omega$

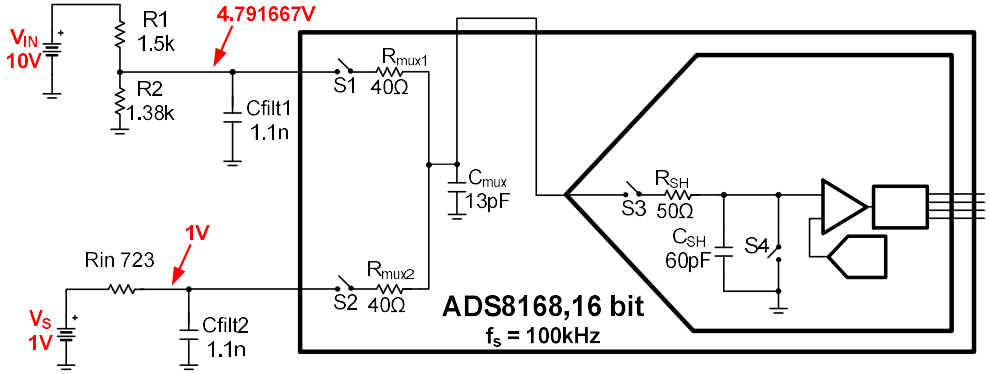
$R_2 := \left(\frac{V_{in}}{V_{in} - V_{adc}}\right) \cdot R_{in} = 1.39074\ k\Omega$

$R_1 := \left(\frac{V_{in} - V_{adc}}{V_{adc}}\right) \cdot R_2 = 1.50663\ k\Omega$

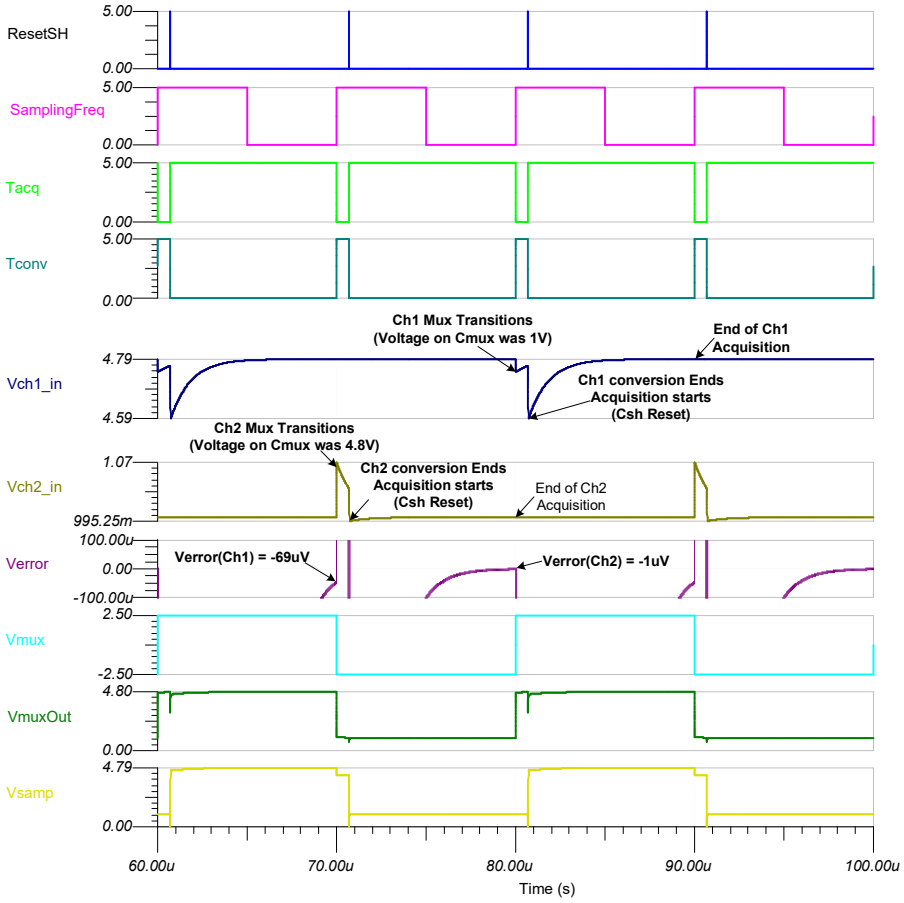
$Half\_LSB := \frac{5\ V}{2 \cdot 2^{16}} = 38.147\ \mu V$



Multiplexed inputs - Signals



- In multiplexed systems there is two switched capacitor circuits (the Mux, and the ADC sample-and-hold).
- The mux parasitic capacitance, C_{mux}, charges to the previous channels voltage
- The sample-and-hold will either be discharged at end of each conversion period, or will retain the previous channel voltage
- A conservative solution is to assume sample and hold fully discharges at end of each conversion period.
- The simulation results show errors of -69uV and 1uV
- The simulation also highlights the transients from the mux switching and from the ADC sample-and-hold



Derivation of Equations

$$V(t) = (V_{final} - V_{initial})\left(1 - e^{-t/\tau}\right) + V_{initial}$$

General Equation for Charging Capacitor with initial condition

$$V_{fs} - \frac{V_{fs}}{2 \cdot 2^N} = \left(V_{fs} - \frac{C_{filt}}{C_{filt} + C_{sh}} V_{fs}\right) \cdot \left(1 - e^{-t/\tau}\right) + \frac{C_{filt}}{C_{filt} + C_{sh}} V_{fs}$$

Substitute initial condition, and final voltage

$$1 - \frac{1}{2 \cdot 2^N} = \left(1 - \frac{C_{filt}}{C_{filt} + C_{sh}}\right) \cdot \left(1 - e^{-t/\tau}\right) + \frac{C_{filt}}{C_{filt} + C_{sh}}$$

$$1 - \frac{1}{2 \cdot 2^N} - \frac{C_{filt}}{C_{filt} + C_{sh}} = \left(1 - \frac{C_{filt}}{C_{filt} + C_{sh}}\right) \cdot \left(1 - e^{-t/\tau}\right)$$

$$1 - \frac{1}{2 \cdot 2^N} - \frac{C_{filt}}{C_{filt} + C_{sh}} = 1 - e^{-t/\tau} - \frac{C_{filt}}{C_{filt} + C_{sh}} + \frac{C_{filt}}{C_{filt} + C_{sh}} \cdot e^{-t/\tau}$$

$$-\frac{1}{2 \cdot 2^N} = -e^{-t/\tau} + \frac{C_{filt}}{C_{filt} + C_{sh}} \cdot e^{-t/\tau}$$

Algebra to solve for t

$$e^{-t/\tau} = \frac{\frac{1}{2 \cdot 2^N}}{\frac{C_{filt}}{C_{filt} + C_{sh}}}$$

$$t = \tau \cdot \ln\left(\frac{2 \cdot 2^N \cdot C_{sh}}{C_{filt} + C_{sh}}\right)$$

Final equation

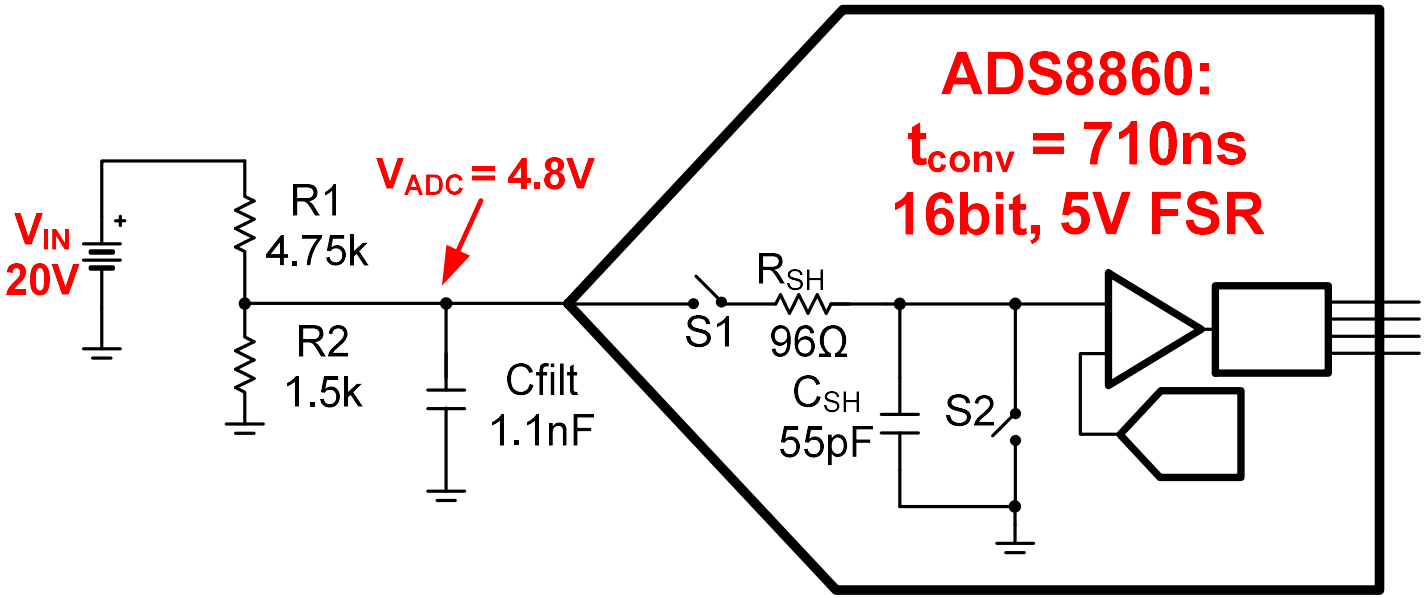
Initial condition on Capacitor. After switch is closed, the fully charged external capacitor (C_{filt}), redistributes charge with the internal capacitor (C_{sh}). This charge exchange results in a droop in voltage.

$$V_{initial} = \frac{C_{ext}}{C_{filt} + C_{sh}} \cdot V_{fs}$$

Thanks for your time!
Please try the quiz.

Questions: EOS and ESD on ADC

1. For the circuit shown below, what sampling rate could be used to achieve ½ LSB settling?
   a. 22kHz
   b. 82kHz
   c. 173kHz
   d. 540kHz



Questions: EOS and ESD on ADC

1. For the circuit shown below, what sampling rate could be used to achieve ½ LSB settling?
   a. 22kHz
   b. 82kHz
   c. 173kHz
   d. 540kHz

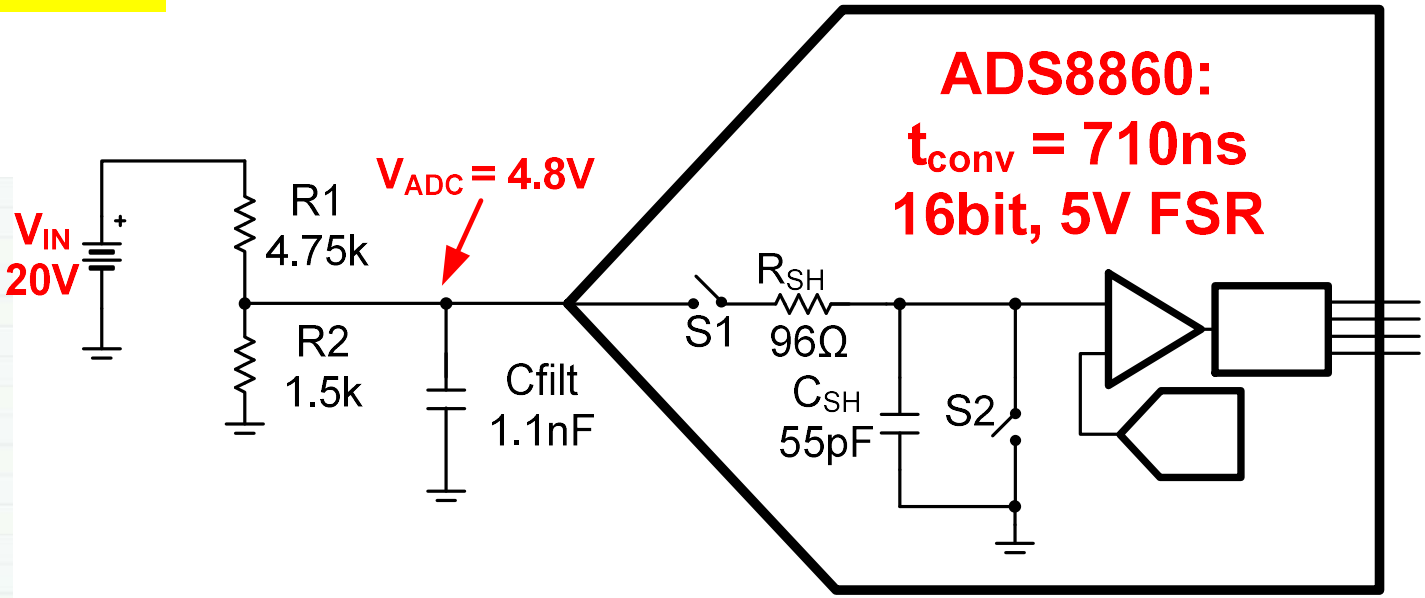
$C_{filt} := 1.1\ nF$ $C_{sh} := 55\ pF$

$N := 16$ $t_{conv} := 710\ ns$

$$R_{in} := \frac{4.75\ k\Omega \cdot 1.5\ k\Omega}{4.75\ k\Omega + 1.5\ k\Omega} = 1.14\ k\Omega$$

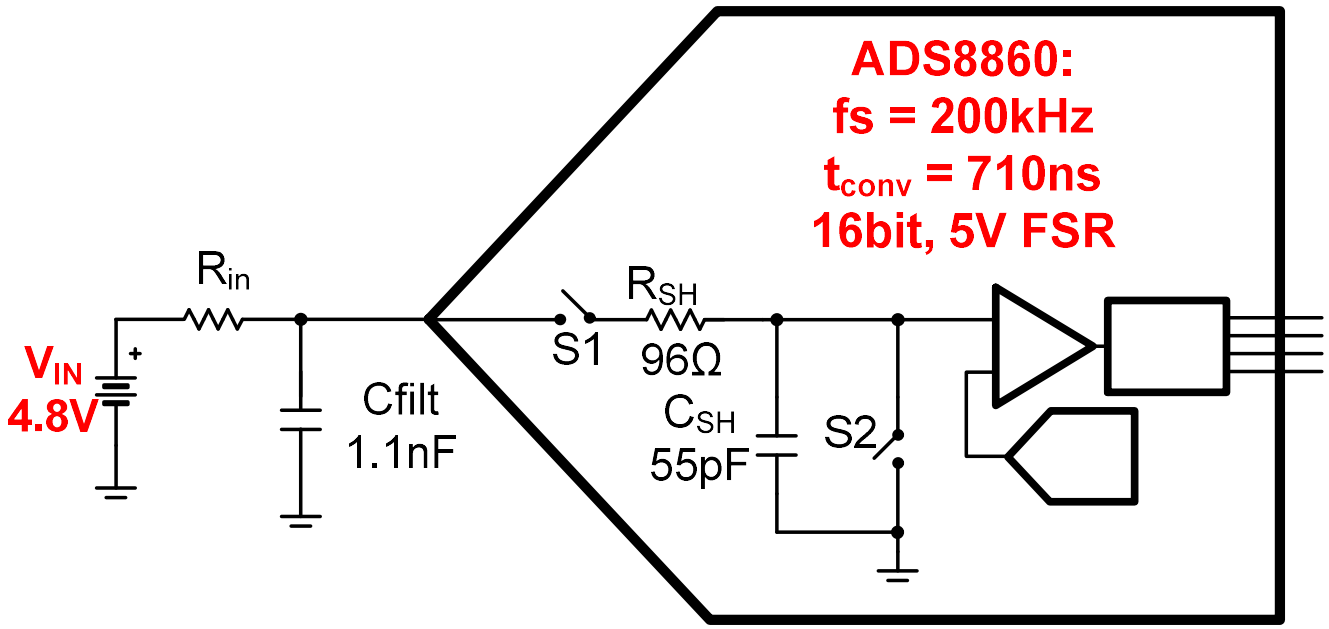
$$t := R_{in} \cdot (C_{filt} + C_{sh}) \cdot \ln\left(\frac{2 \cdot 2^N \cdot C_{sh}}{C_{filt} + C_{sh}}\right) = 11.507\ \mu s$$

$$f_s := \frac{1}{t + t_{conv}} = 81.856\ kHz$$



Questions: EOS and ESD on ADC

2. For the circuit shown below, what is the maximum input resistance, Rin, that will allow a 200kHz sampling rate and ½ LSB settling error?
   a. 121Ω
   b. 222Ω
   c. 425Ω
   d. 744Ω
   e. 1.24kΩ



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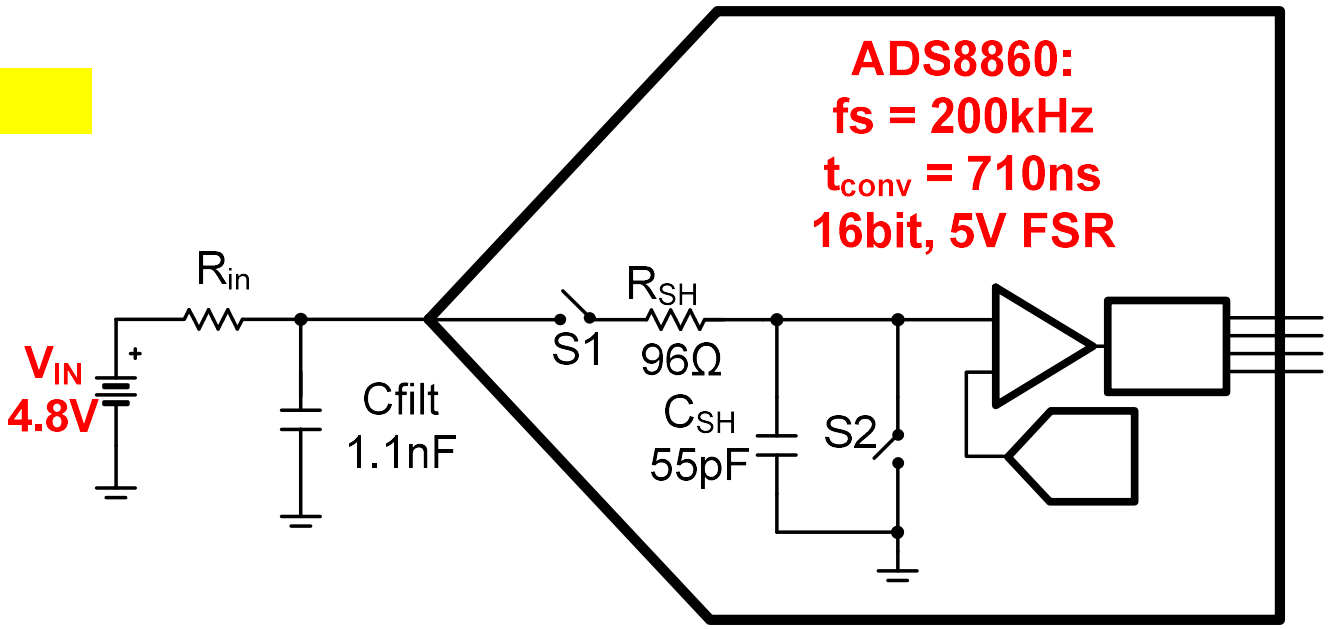
   e. 1.24kΩ

$C_{sh} := 55\ pF$ $t_{ConvMax} := 710\ ns$

$f_s := 200\ kHz$ $C_{ext} := 1.1\ nF$

$$t_{AcqMin} := \frac{1}{f_s} - t_{ConvMax} = 4.29\ \mu s$$

$$R_{in} := \frac{t_{AcqMin}}{(C_{ext}+C_{sh}) \cdot \ln\left(\frac{2 \cdot 2^{16} \cdot C_{sh}}{C_{ext}+C_{sh}}\right)} = 0.425\ k\Omega$$



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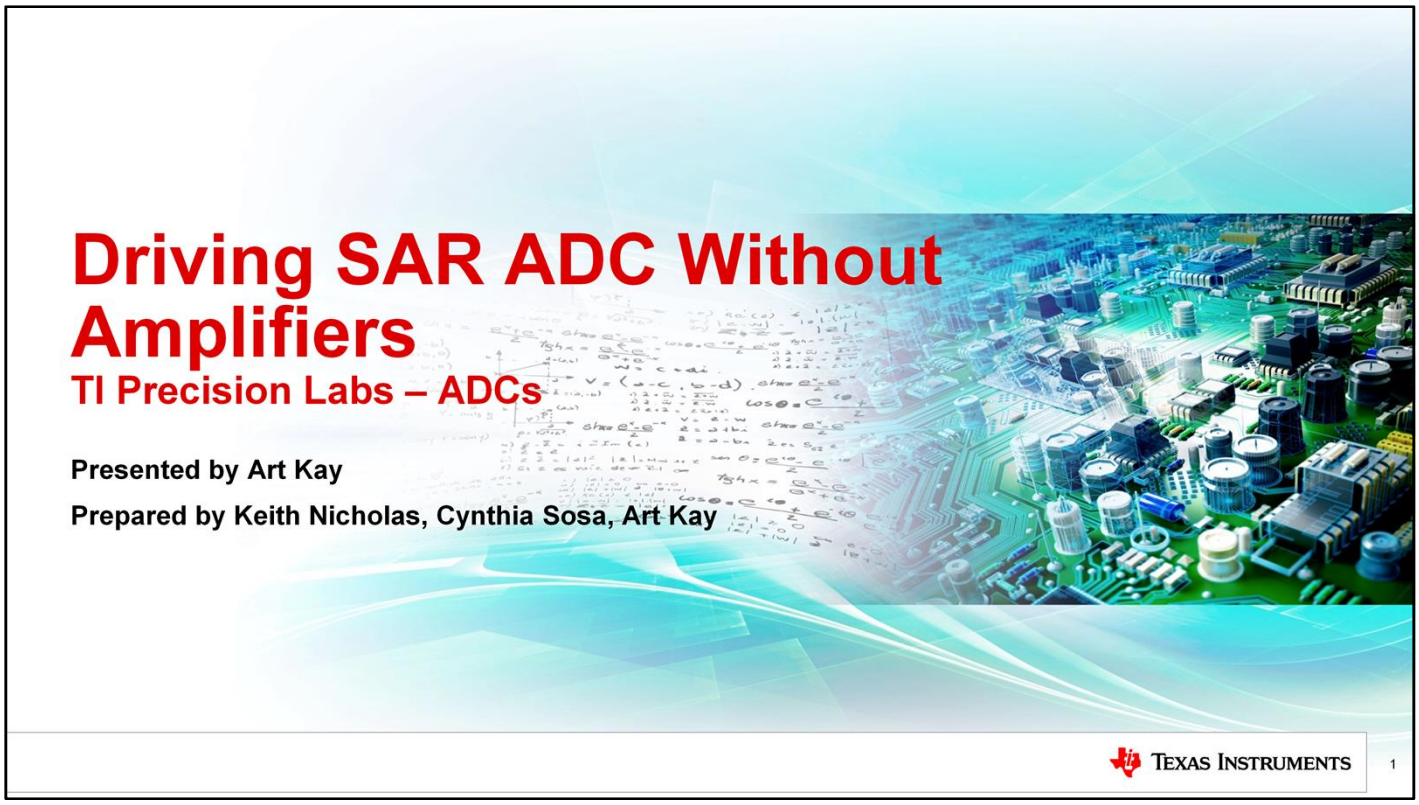

Hello and welcome to the TI Precision Labs Section on Driving SAR ADC without amplifiers. Some common examples of SAR ADC usage without amplifiers are monitoring power supplies or monitoring a slow moving sensor such as a thermistor. In previous videos we learned how to select the amplifier and external RC filter to achieve good settling. In these videos we used simulation and a parametric search to find the optimal RC value. Although this method can be used on circuits without amplifiers, it is much easier to use some simple equations to select the values. The reason the simple equations can be used here but not for circuits using amplifier drive is that circuits without amplifiers are simple first order circuits and amplifier circuits are higher

order more complex systems. The higher order systems are difficult to model mathematically as they depend on many factors such as gain and output load. The first order system on the other hand has a simple mathematical solution that yields a set of equations that can be used to find the RC filter and sampling rate needed for proper settling.

Find sampling rate: ADC without buffer amplifier

General Equations for Sampling Rate given a source impedance Rin to achieve 1/2 LSB settling accuracy

$$C_{filt} = 20 \cdot C_{sh}$$

$$t_{AcqMin} = R_{in} \cdot (C_{filt} + C_{sh}) \cdot ln\left(\frac{2 \cdot 2^N \cdot C_{sh}}{C_{filt} + C_{sh}}\right)$$

$$f_s = \frac{1}{t_{AcqMin} + t_{ConvMax}}$$

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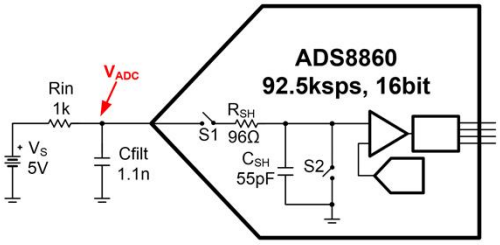
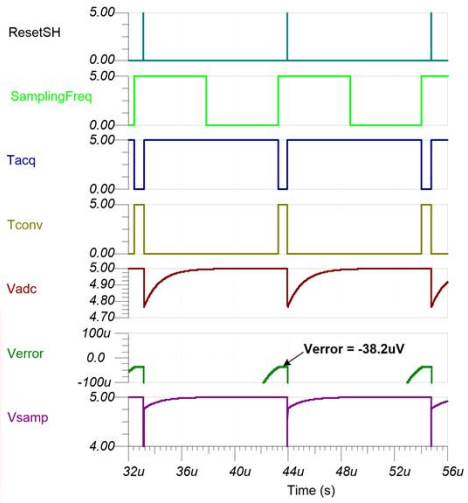
$$f_s := \frac{1}{t_{AcqMin} + t_{ConvMax}} = 92.562\ kHz$$

$$Half\_LSB := \frac{V_{fs}}{2 \cdot 2^N} = 38.147\ \mu V$$

$$f_c := \frac{1}{2 \cdot \pi \cdot R_{in} \cdot C_{filt}} = 144.686\ kHz$$





- This procedure assumes that Rin is known
- Rin may be the source impedance of the sensor.
- Targeted settling error of 1/2LSB
- Simulated settling error approximately 1/2LSB (1/2LSB = 38.1µV, Sim = 38.2µV)

Texas Instruments 2

Here we show a simple example of how the sampling rate can be selected to achieve good settling error for a SAR ADC without a driver amplifier. Typical use cases for this include monitoring power supply rails, or monitoring sensors like thermistors. The source Vs is modeled as an ideal DC source. In a practical case the source may have significant source impedance. This impedance will need to be included in the input resistance Rin. The input capacitance, Cfilt, is selected in the same way we selected it in previous videos. That is, it is selected by multiplying the internal sample and hold capacitance value by twenty. To find the minimum acquisition period use the equation given here. The acquisition period is used with the specified conversion period to calculate the

sampling rate. This equation is derived at the end of the presentation. For now, just realize that this equation is based on the standard charge for an RC circuit as well as a charge redistribution that happens when the sample and hold is connected to the Cfilt capacitor.

The ADS8860 example shows how to calculate the sampling rate with a full scale input signal and a 1k ohm input impedance. The sample and hold capacitance, conversion period, and resolution are provided from the data sheet. The external filter is selected to be twenty times the sample and hold value, or 1.1nF in this case. Applying all these values to the acquisition period formula yield approximately 10us. This is used with the conversion period to find the sampling rate. Running a simulation on this circuit shows the settling error to be 38.2uV which is very close to half an LSB. Of course, the same results could be determined using the parametric search method described in previous videos, but this method is much simpler. Finally, we calculate the bandwidth of the input filter as this information may be useful to understand how the filter impacts noise rejection. In this case the filter limits the input frequency to 144kHz, so it's not very effective at rejecting noise. We will see additional examples where this frequency is lower but generally this also means a low sampling rate is required.

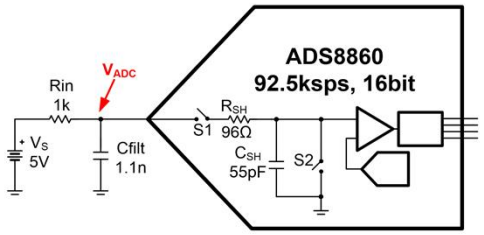
Initial start up time

Initial Settling of RC filter

$N = 16 \quad R_{in} := 1\ k\Omega$

$C_{sh} := 15\ pF \quad C_{filt} := 1.1\ nF$

$t_{settling} := R_{in} \cdot (C_{sh} + C_{filt}) \cdot \ln(2^N) = 9.274\ \mu s$



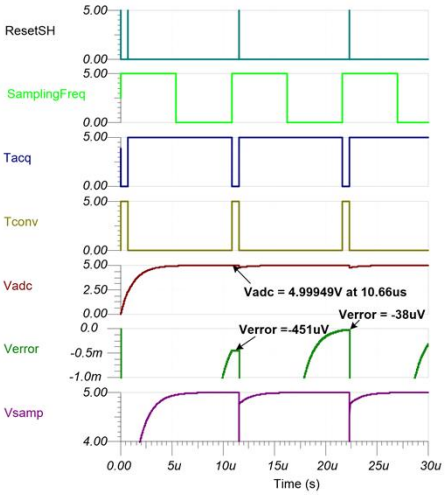


Table 38: Time required to settle to a specified conversion accuracy

Accuracy in bits (N)	Settling time in time constants (N_{TC})	Accuracy in bits (N)	Settling time in time constants (N_{TC})
8	5.5	17	11.78
9	6.24	18	12.48
10	6.93	19	13.17
11	7.62	20	13.86
12	8.32	21	14.56
13	9.01	22	15.25
14	9.70	23	15.94
15	10.40	24	16.64
16	11.04	25	17.33

$N_{TC} = \ln(2^N)$ (201)

- The results on the previous slide assume that the input RC filter is settled.
- The initial settling time requirement can be calculated using the equations shown.
- This equation assumes settling for a resolution requirement.
- The simulation shows that the first sample has worse error due to the start-up charging of the input RC filter

TEXAS INSTRUMENTS 3

It is important to understand that the previous calculation and simulation assume that the input capacitor, Cfilt, is fully changed at the start of the conversion. This will not be true immediately after the system is powered up. The initial power up period can be calculated using the table or equation shown here. The equation is based on the RC time constant and the number of bits of resolution. For a 16 bit converter the initial charge up time for 1 LSB of error is calculated by multiplying by 11.04 from the table, or using the equation.

Looking at the simulation for this example, you can see that Vadc is initially zero and charges exponentially after

power is applied. Also, you can see that the first conversion result has worse error than subsequent conversion. The main point here is to make sure that the initial system power up time is accounted for. This can be done by adding a short delay before taking measurements or accepting the error introduce by this start-up behavior.

Find input source impedance for sampling rate

ADS7047 Example: Find a voltage divider that will settle with 100kHz sampling rate

$C_{sh} := 16\ pF \quad t_{ConvMax} := 250\ ns$

$f_s := 100\ kHz \quad V_{in} := 10\ V \quad V_{adc} := 3.6\ V$

$C_{filt} := 20 \cdot C_{sh} = 320\ pF \quad N := 12$

$t_{AcqMin} := \frac{1}{f_s} - t_{ConvMax} = 9.75\ \mu s$

$R_{in} := \frac{t_{AcqMin}}{(C_{filt} + C_{sh}) \cdot \ln\left(\frac{2 \cdot 2^N \cdot C_{sh}}{C_{filt} + C_{sh}}\right)} = 4.864\ k\Omega$

$R_{in} = \frac{R_1 \cdot R_2}{R_1 + R_2} = 4.864\ k\Omega$

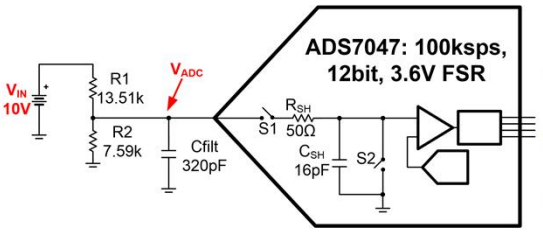
$V_{adc} = \frac{R_2 \cdot 10\ V}{R_1 + R_2} = 3.6\ V$

Solve for R1, R2

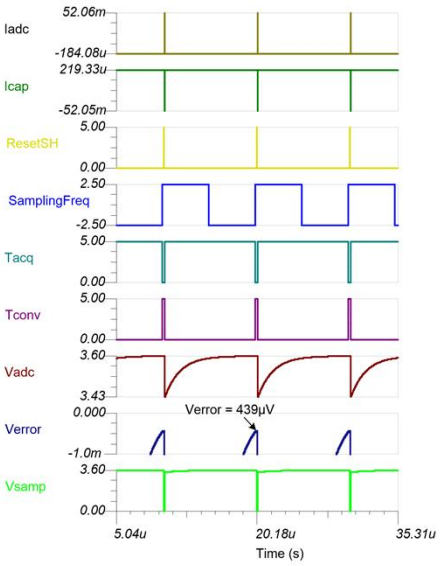
$R_2 := \left(\frac{V_{in}}{V_{in} - V_{adc}}\right) \cdot R_{in} = 7.599\ k\Omega$

$R_1 := \left(\frac{V_{in} - V_{adc}}{V_{adc}}\right) \cdot R_2 = 13.51\ k\Omega$

$Half\_LSB := \frac{3.6\ V}{2 \cdot 2^N} = 439.453\ \mu V$



- This procedure assumes a desired sampling rate, and solves for the required source impedance (Rin)
- The source impedance for the voltage divider is the parallel combination of R1 and R2
- Settling Error matches the expected error (1/2LSB = 439µV, Sim = 439µV)



TEXAS INSTRUMENTS 4

Some designs may have a specific sampling rate requirement, but have flexibility on the source impedance selection. A typical example of this would be monitoring the supply using a voltage divider. In the case of the voltage divider the main factor in selecting the divider impedance is often power dissipation. Choosing a lower impedance divider will increase power dissipation, but will also allow for a faster sampling rate. The equations here are rearranged to solve for maximum input resistance to achieve a particular sampling rate.

In this example the goal is to achieve a 100kHz sampling rate. The converter is a 12 bit device with a 3.6V full scale range. Applying this information to the equation

yields an input resistance of 4.86k ohm. The voltage divider here is intended to divide the 10V input signal to the 3.6V full scale range. From the perspective of the ADC input the two resistors R1 and R2 are in parallel and this parallel resistance needs to be equal to the calculated input resistance. These two equations can be solved for R1 and R2 as shown. In this example, R2 and R1 are 7.59k and 13.51k respectively. These equations are generic and can be used for similar SAR ADC voltage monitor problems. Notice that the error shown in the simulation results is very close to the expected error of one half LSB.

Periodic single-shot conversions

General Equations for recovery period for 1/2 LSB settling on single shot conversion.

$$C_{filt} = 2 \cdot 2^N \cdot C_{sh}$$

$$t_1 = R_{in} \cdot (C_{filt} + C_{sh}) \cdot ln(2)$$

$$t_{recovery} = t_1 + t_{ConvMax}$$

ADS7042 Example

$R_{in} := 100\ k\Omega \quad C_{sh} := 15\ pF$

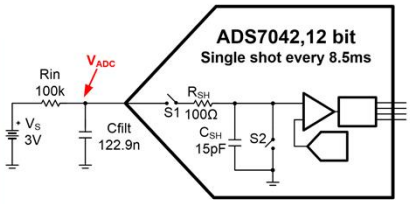
$t_{ConvMax} := 800\ ns \quad N := 12$

$C_{filt} := 2 \cdot 2^N \cdot C_{sh} = 122.88\ nF$

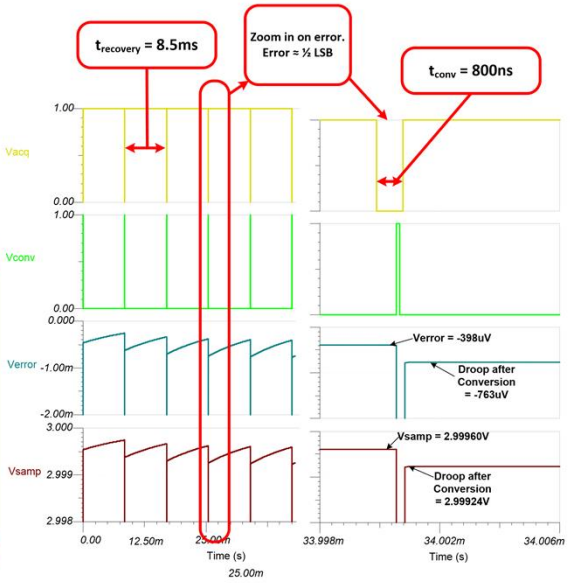
$t_1 := R_{in} \cdot (C_{filt} + C_{sh}) \cdot \ln(2) = 8.518\ ms$

$t_{recovery} := t_1 + t_{ConvMax} = 8.519\ ms$

$Half\_LSB := \frac{3\ V}{2 \cdot 2^{12}} = 366.211\ \mu V$



- This procedure assumes a fast single-shot conversion is done periodically
- The capacitor is selected to so that error is 1 LSB at start of acquisition period
- The recovery time is set so that the error is ½ LSB at start of conversion.
- Simulated settling error approximately 1/2LSB (1/2LSB = 366µV, Sim = 398µV)

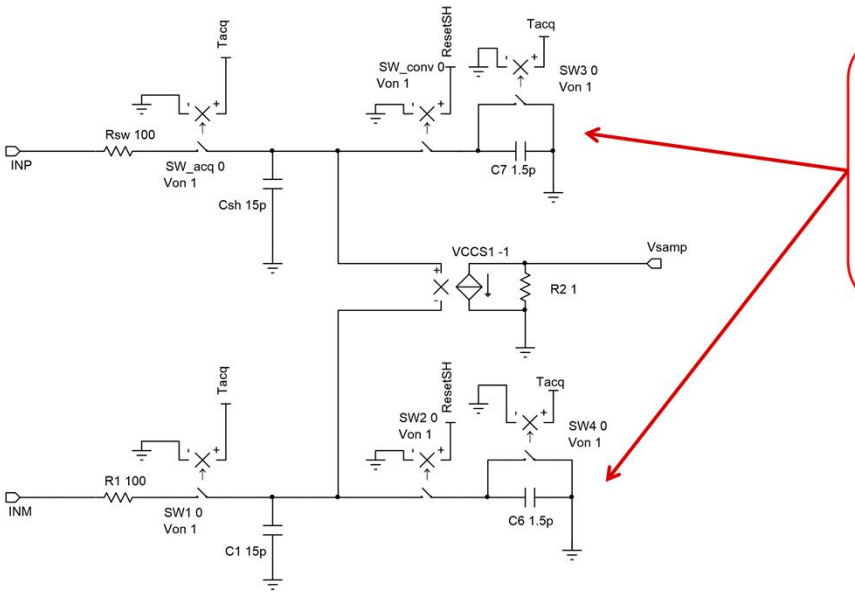


Some system monitoring solutions only need to periodically monitor the supplies. So, for example, a converter may take a quick single conversion at 1Msps once every hundred milliseconds. For this kind of solution a very large filter capacitor is often used on the ADC input. The capacitor is significantly larger than the sample-and-hold capacitor so that at the start of the conversion cycle the droop introduced is minimal. The design equations shown here select a filter capacitor that will introduce one half LSB of droop error at the start of the conversion cycle. The next equation calculates a recovery time that you would have to wait between single-shot conversions. The main advantage of this technique is that it has minimal impact on the

microcontroler processing overhead. Furthermore, this method can be applied to multiplexed devices so that a periodic scan of all the multiplexer inputs can be used to read all the system monitor voltages.

In this example a large 100k source impedance is used with a full scale 3V signal. The external Cfilt capacitor is selected to be 122nF using the equation to introduce one half LSB error at the start of the conversion period. Applying the values to the relationship yields a recovery time of 8.5ms. Simulations show that the error is comparable with the expected half LSB of error.

Is the sample and hold completely reset?



The reset capacitors deplete the charge on the sample and hold capacitor by 10% at end of conversion cycle. The old model reset to zero. Assuming the input signal is DC, the input capacitor looks like an effective capacitance of 1.5pF in this example.

Up to this point all the material we have presented on SAR ADC modeling has assumed that the sample and hold capacitor is completely reset at the end of each conversion. In most practical SAR ADC this is not true. In fact, at the end of each conversion cycle some amount of change will be depleted on the sample and hold capacitor, but it will generally not be fully discharged. This means that the actual settling is typically better than predicted by the model that we have been using. The model shown here illustrates a case where the sample-and-hold charge is depleted by 10% at the end of each conversion cycle. Notice that the section of the model that previously shorted the sample-and-hold capacitor to ground is replaced with a “reset” capacitor that is equal

to 10% of the sample and hold capacitor. Unfortunately, all SAR ADC do not behave the same way and the amount of post conversion droop will differ for different devices. Furthermore, this information is normally not specified in the ADC data sheet. It is possible to measure this effect and use this information in the simulation of circuits. However, designing based on the conservative approach will always yield good results. Also, as we will discuss in the next slide, the conservative approach is best for multiplexed devices as the sample and hold capacitor of subsequent channels will charge to different voltage levels.

Multiplexed inputs – Component selection

ADS8168 Example: Find a voltage divider that will settle with 100kHz sampling rate

$C_{sh} := 60\ pF \quad t_{ConvMax} := 600\ ns$

$N := 16 \quad C_{mux} := 13\ pF$

$f_s := 100\ kHz \quad V_{in} := 10\ V \quad V_{adc} := 4.8\ V$

$C_{filt} := 20 \cdot (C_{sh} + C_{mux}) = 1.46\ nF$

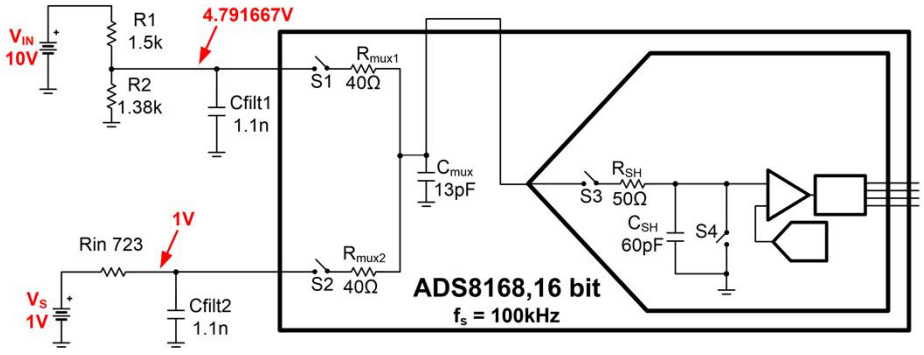
$t_{AcqMin} := \frac{1}{f_s} - t_{ConvMax} = 9.4\ \mu s$

$R_{in} := \frac{t_{AcqMin}}{(C_{filt} + C_{sh}) \cdot \ln\left(\frac{2 \cdot 2^N \cdot C_{sh}}{C_{filt} + C_{sh}}\right)} = 0.723\ k\Omega$

$R_2 := \left(\frac{V_{in}}{V_{in} - V_{adc}}\right) \cdot R_{in} = 1.39074\ k\Omega$

$R_1 := \left(\frac{V_{in} - V_{adc}}{V_{adc}}\right) \cdot R_2 = 1.50663\ k\Omega$

$Half\_LSB := \frac{5\ V}{2 \cdot 2^{16}} = 38.147\ \mu V$

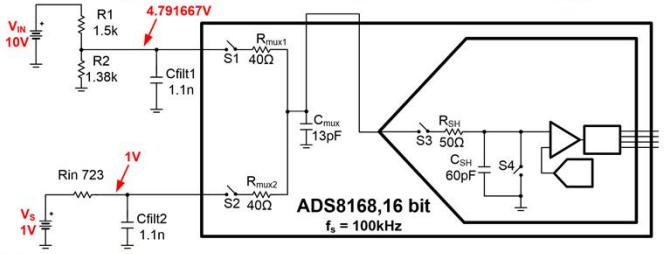


This example shows a typical multiplexed system. The multiplexer model contains FET switches, the switch on-resistance, the switch parasitic capacitance, and the SAR ADC model. In this example, we only show two channels, but the same principles can be applied to multiplexers with more channels. When the multiplexer switches channels, the parasitic capacitance behaves very similar to a sample and hold circuit. In this example, when switch S1 is closed, the mux capacitor will charge up to approximately 4.79V. When the multiplexer changes channels and S2 closes the 1V input will have to discharge the stored 4.79V charge from the previous channel. Furthermore, the ADC itself still has a sample and hold settling, and for each conversion cycle the ADC may need

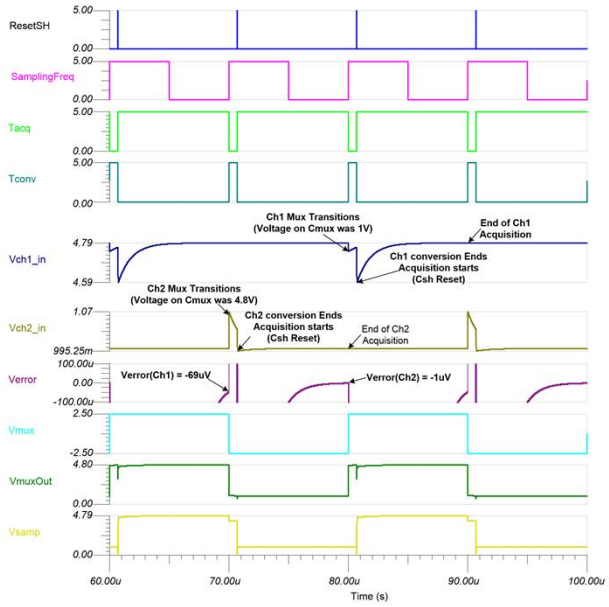
to settle to a different voltage. In this example the ADC will alternate from 4.79V to 1V. Since each conversion cycle can have a different voltage, it doesn't really matter if the ADC sample and hold is fully discharged during each conversion cycle. For this reason the conservative ADC model is normally used for multiplexed cases.

The equations used here are the same as the previous equations except that the multiplexer parasitic capacitance is included. In this example, the required input impedance of 732 ohms is calculated to achieve a 100kHz sampling rate. Note that each channel needs to have a maximum of 732 ohms impedance or the channel will have settling errors. Of course, if this impedance is too low from a power perspective, the sampling rate could be adjusted to a lower frequency.

Multiplexed inputs - Signals



- In multiplexed systems there is two switched capacitor circuits (the Mux, and the ADC sample-and-hold).
- The mux parasitic capacitance, C_{mux}, charges to the previous channels voltage
- The sample-and-hold will either be discharged at end of each conversion period, or will retain the previous channel voltage
- A conservative solution is to assume sample and hold fully discharges at end of each conversion period.
- The simulation results show errors of -69uV and 1uV
- The simulation also highlights the transients from the mux switching and from the ADC sample-and-hold



This slide shows the simulation results for the example from the previous page. For each conversion there are two transients: One transient occurs where the mux changes channels causing the parasitic mux capacitance to charge. Another transient occurest where the converter starts it's acquisition period. Looking at Vch1_in you can see the transient from changing the mux channel is relatively small. This transient occurs as the mux capacitance was previously changed to 1V from the previous channel. When the acquisition period starts the internal 60pF sample and hold capacitance is initially discharged so the voltage on Cfilt1 droops significantly. The same type of transient can be seen on channel 2. Looking at the error for both channels 1 and 2 you can

see that the worst case error is about 69uV. Half of one LSB error is 38uV, so this error is closer to 1 LSB. This is not surprising as the multiplexer adds an extra settling transient from when the channels are changed. In all of these examples adding some extra margin can be achieved by choosing a lower sampling rate or reducing the input impedance.

Derivation of Equations

$$V(t) = (V_{final} - V_{initial})\left(1 - e^{-t/\tau}\right) + V_{initial}$$

General Equation for Charging Capacitor with initial condition

$$V_{fs} - \frac{V_{fs}}{2 \cdot 2^N} = \left(V_{fs} - \frac{C_{filt}}{C_{filt} + C_{sh}} V_{fs}\right) \cdot \left(1 - e^{-t/\tau}\right) + \frac{C_{filt}}{C_{filt} + C_{sh}} V_{fs}$$

Substitute initial condition, and final voltage

$$1 - \frac{1}{2 \cdot 2^N} = \left(1 - \frac{C_{filt}}{C_{filt} + C_{sh}}\right) \cdot \left(1 - e^{-t/\tau}\right) + \frac{C_{filt}}{C_{filt} + C_{sh}}$$

$$1 - \frac{1}{2 \cdot 2^N} - \frac{C_{filt}}{C_{filt} + C_{sh}} = \left(1 - \frac{C_{filt}}{C_{filt} + C_{sh}}\right) \cdot \left(1 - e^{-t/\tau}\right)$$

$$1 - \frac{1}{2 \cdot 2^N} - \frac{C_{filt}}{C_{filt} + C_{sh}} = 1 - e^{-t/\tau} - \frac{C_{filt}}{C_{filt} + C_{sh}} + \frac{C_{filt}}{C_{filt} + C_{sh}} \cdot e^{-t/\tau}$$

$$-\frac{1}{2 \cdot 2^N} = -e^{-t/\tau} + \frac{C_{filt}}{C_{filt} + C_{sh}} \cdot e^{-t/\tau}$$

$$e^{-t/\tau} = \frac{\frac{1}{2 \cdot 2^N}}{\frac{C_{filt}}{C_{filt} + C_{sh}}}$$

Algebra to solve for t

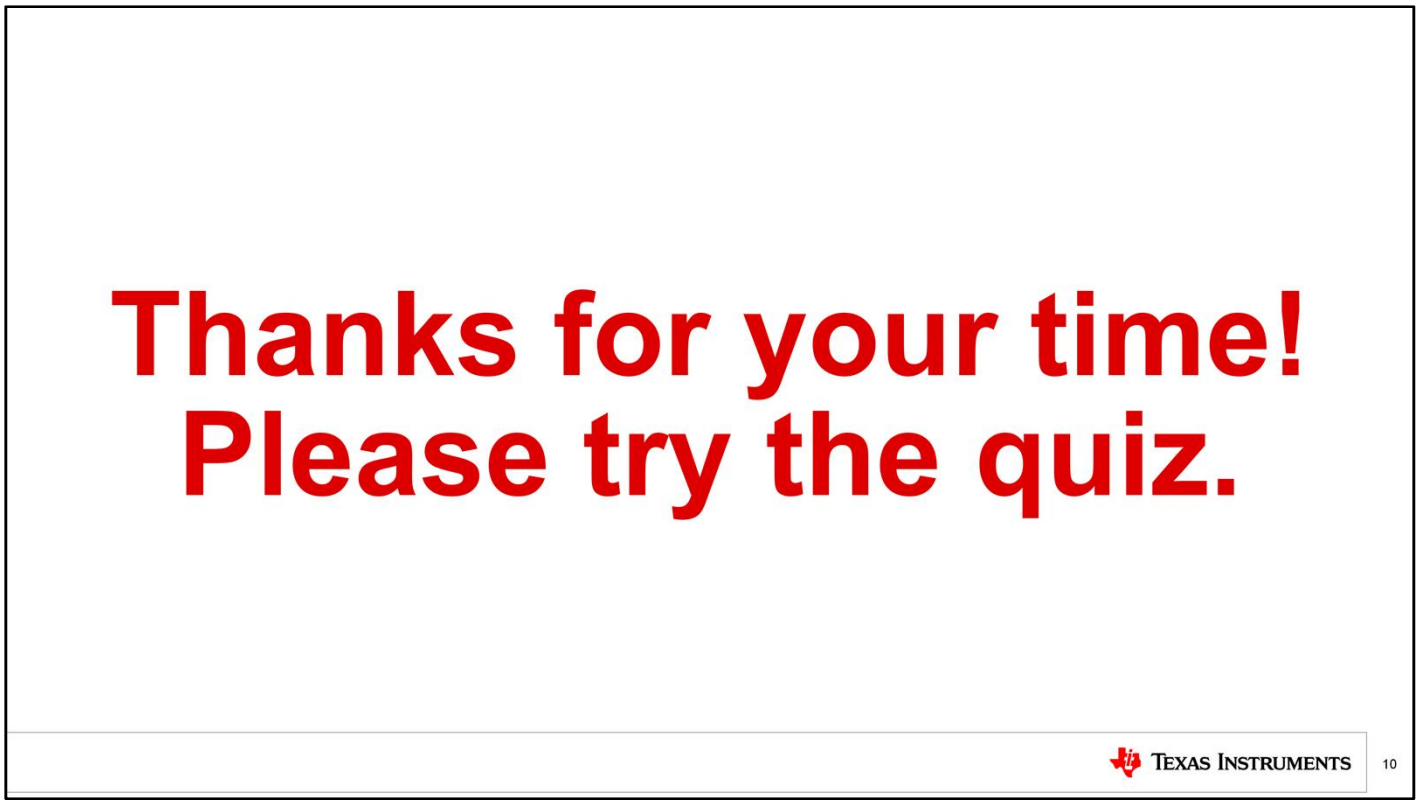
$$t = \tau \cdot \ln\left(\frac{2 \cdot 2^N \cdot C_{sh}}{C_{filt} + C_{sh}}\right)$$

Final equation

Initial condition on Capacitor. After switch is closed, the fully charged external capacitor (C_{filt}), redistributes charge with the internal capacitor (C_{sh}). This charge exchange results in a droop in voltage.

$$V_{initial} = \frac{C_{ext}}{C_{filt} + C_{sh}} \cdot V_{fs}$$

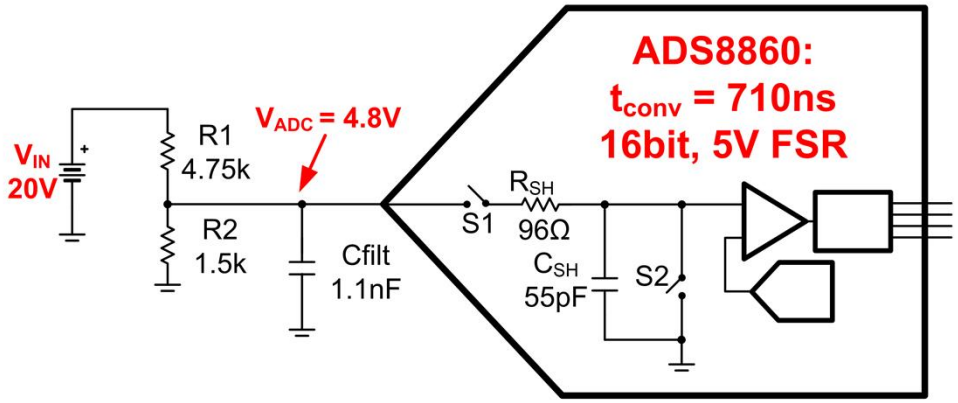
The last slide shows the derivation of the equation used in this presentation. The first equation is the generic equation for and RC change curve with an initial contention. The second equation substitutes in the initial condition. The initial condition can be derived by considering the voltage droop introduced when the fully discharged sample-and-hold capacitator is put in parallel with the fully changed external filter capacitor. The final voltage in the second equation assumes a half LSB of droop from full scale. After substituting the initial condition some algebra is used to solve for time.



That concludes this theory part of the video – thank you for watching! Keep watching to and try the quiz and check your understanding of this video's content.

Questions: EOS and ESD on ADC

1. For the circuit shown below, what sampling rate could be used to achieve ½ LSB settling?
   a. 22kHz
   b. 82kHz
   c. 173kHz
   d. 540kHz



Question 1, For the circuit shown below, what sampling rate could be used to achieve ½ LSB settling?

Questions: EOS and ESD on ADC

1. For the circuit shown below, what sampling rate could be used to achieve ½ LSB settling?
   a. 22kHz
   b. 82kHz
   c. 173kHz
   d. 540kHz

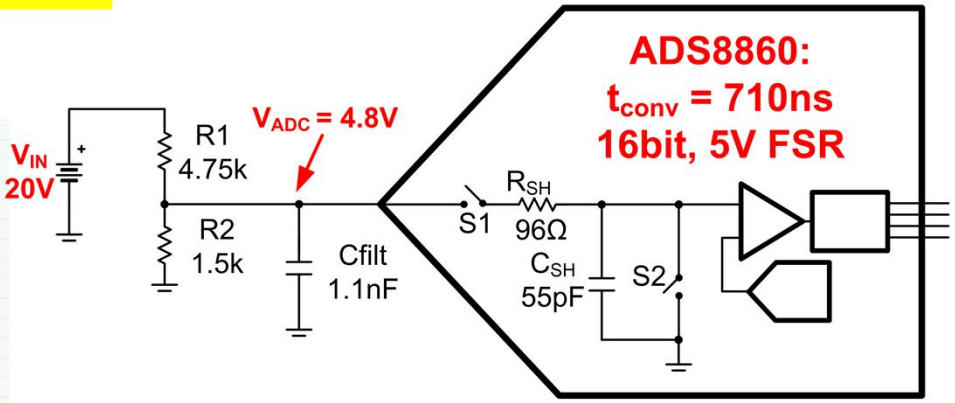
$C_{filt} := 1.1\ nF$ $C_{sh} := 55\ pF$

$N := 16$ $t_{conv} := 710\ ns$

$$R_{in} := \frac{4.75\ k\Omega \cdot 1.5\ k\Omega}{4.75\ k\Omega + 1.5\ k\Omega} = 1.14\ k\Omega$$

$$t := R_{in} \cdot (C_{filt} + C_{sh}) \cdot \ln\left(\frac{2 \cdot 2^N \cdot C_{sh}}{C_{filt} + C_{sh}}\right) = 11.507\ \mu s$$

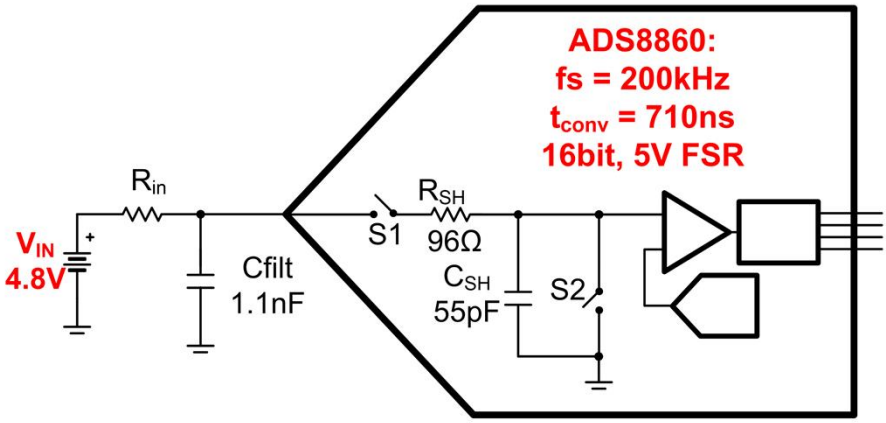
$$f_s := \frac{1}{t + t_{conv}} = 81.856\ kHz$$



The correct answer is “b. 82kHz”. The input impedance is the parallel combination of R1 and R2. This is used with the settling equation to find the acquisition period and finally the sampling rate.

Questions: EOS and ESD on ADC

2. For the circuit shown below, what is the maximum input resistance, Rin, that will allow a 200kHz sampling rate and ½ LSB settling error?
   a. 121Ω
   b. 222Ω
   c. 425Ω
   d. 744Ω
   e. 1.24kΩ



Question 2, For the circuit shown below, what is the maximum input resistance, Rin, that will allow a 200kHz sampling rate and ½ LSB settling error?

Questions: EOS and ESD on ADC

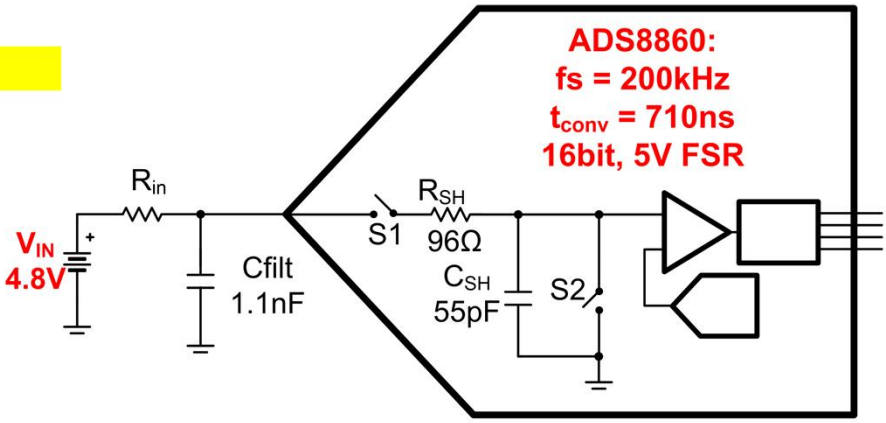
2. For the circuit shown below, what is the maximum input resistance, Rin, that will allow a 200kHz sampling rate and ½ LSB settling error?
   a. 121Ω
   b. 222Ω
   c. 425Ω
   d. 744Ω
   e. 1.24kΩ

$C_{sh} := 55\ pF$ $t_{ConvMax} := 710\ ns$

$f_s := 200\ kHz$ $C_{ext} := 1.1\ nF$

$$t_{AcqMin} := \frac{1}{f_s} - t_{ConvMax} = 4.29\ \mu s$$

$$R_{in} := \frac{t_{AcqMin}}{(C_{ext} + C_{sh}) \cdot \ln\left(\frac{2 \cdot 2^{16} \cdot C_{sh}}{C_{ext} + C_{sh}}\right)} = 0.425\ k\Omega$$



The correct answer is “c. 425 ohms”. In this case the formula is rearranged to solve for Rin.

That concludes this video – thank you for watching!